

THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, 2012 ALL RIGHT RESERVED.

HSF Property: ROHS or Halogen-Free

COMET DIS

SI1 BUILD

2012.11.30

21-OCT-2002		
DATE	CHANGE NO.	REV

INVENTEC					
DRAWER	EE	DATE	POWER	DATE	
DESIGN	isa chen	2012/10/24	isa chen	2012/10/24	
CHECK	isa chen	2012/10/24	isa chen	2012/10/24	
RESPONSIBLE	isa chen	2012/10/24	isa chen	2012/10/24	
SIZE: A4					VER: x01
FILE NAME: COMET DIS					SIZE: 5
PIN: xxxxxxxxxxxx					CODE: CS
					DOC NUMBER: 6310xxxx-0-0
					REV: x01
					SHEET: 1 of 17

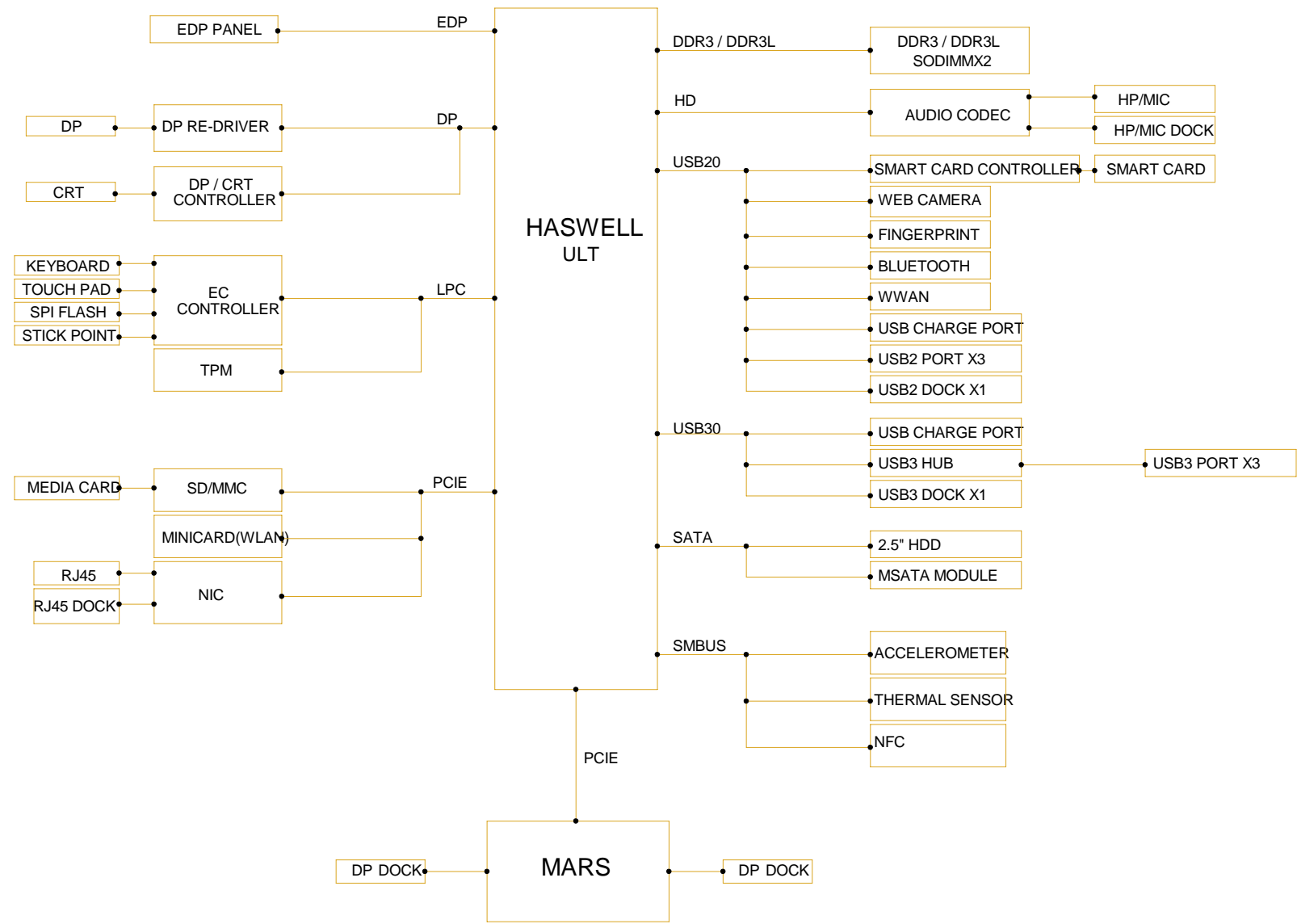
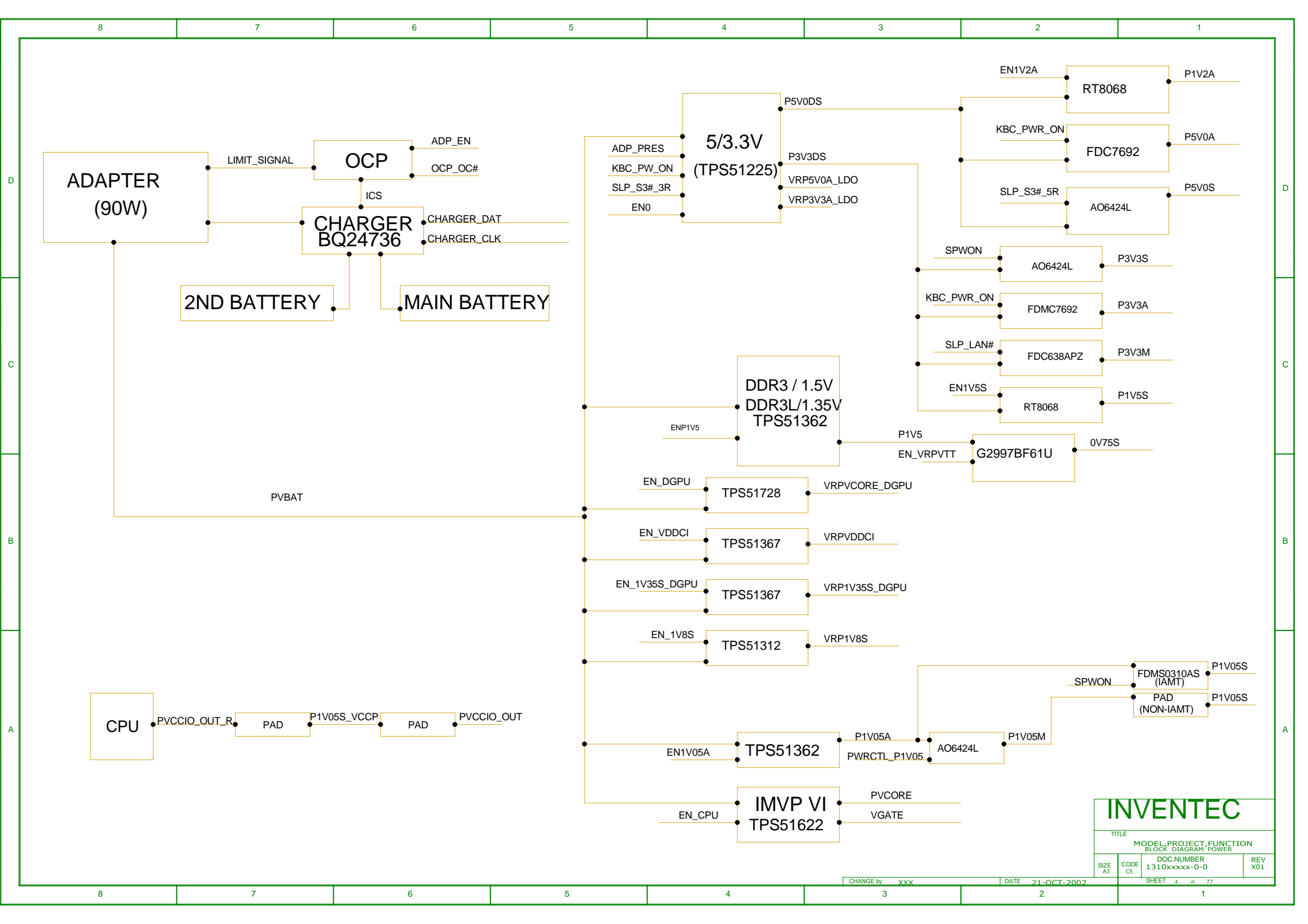
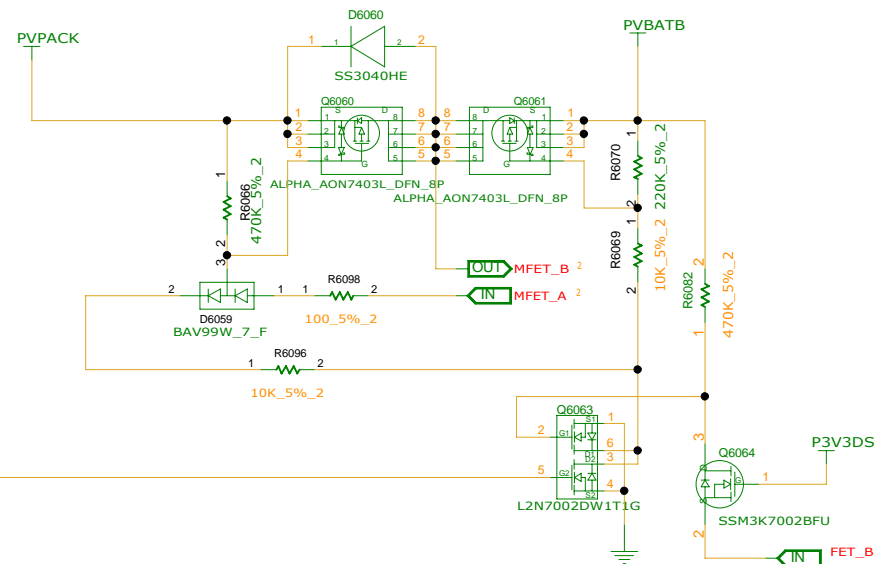
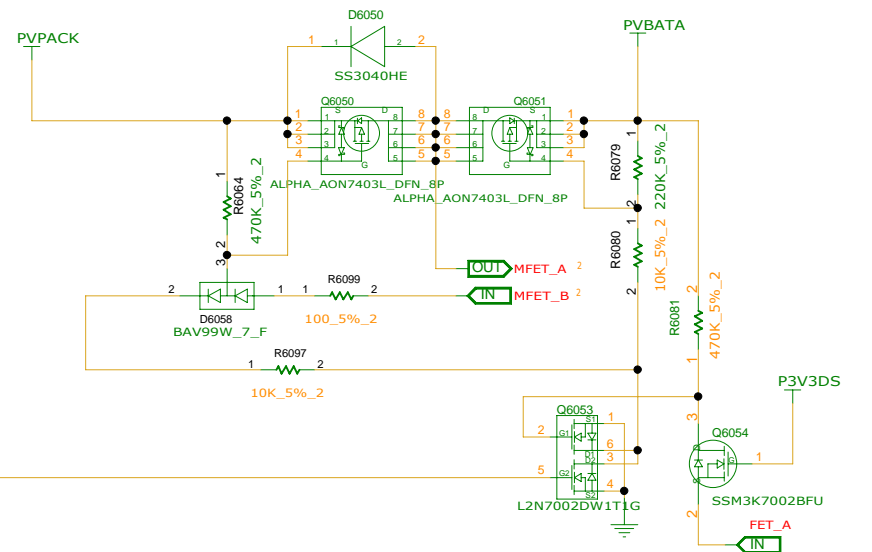
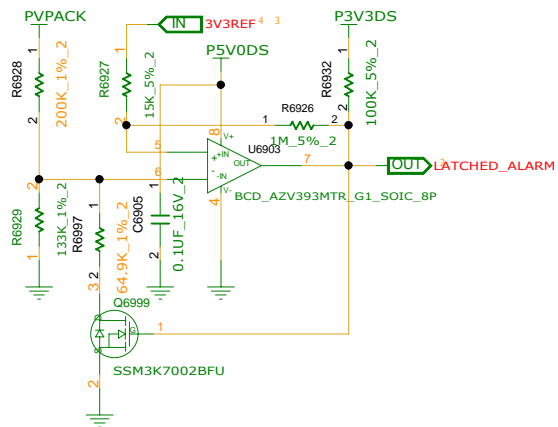


TABLE OF CONTENTS

01.PROJECT NAME	26.XDP & ME CONN.	51.KBC, SPI
02.BLOCK DIAGRAM	27.HASWELL_1 (MISC,JTAG)	52.KEYBOARD
03.TABLE OF CONTENTS	28.HASWELL_2 (LPC,SPI,SMBUS,CLINK,PM)	53.TPM
04.POWER BLOCK DIAGRAM	29.HASWELL_3 (GPIO)	54.LAN
05.SYSTEM POWER(CHARGER)	30.HASWELL_4 (DP,EDP)	55.WLAN/BT SLOT
06.SYSTEM POWER(BATT SELECTOR)	31.HASWELL_5 (DDR)	56.WWAN SLOT, SIM SLOT
07.SYSTEM POWER(OCF)	32.HASWELL_6 (PCIE,USB)	57.DOCKING
08.SYSTEM POWER(P3V3A&P5V0A)	33.HASWELL_7 (RTC,AUDIO,SATA,JTAG)	58.B TO B CONN, POINT STICK CONN
09.P3V3A&P5V0A_CHG PORT	34.HASWELL_8 (CLK)	59.AUDIO CODEC
10.SYSTEM POWER(P1V5)	35.HASWELL_9 (POWER)	60.AUDIO JACK, MIC AMP.
11.SYSTEM POWER(P1V05_M)	36.HASWELL_10 (POWER)	61.CARD READER
12.SYSTEM POWER(P1V05S)	37.HASWELL_11 (GND)	62.BUTTON, LED
13.USB HUB POWER (P1V2A)	38.SYSTEM MEMORY (DIMM0)	63.SMART CARD DAUGHTER BOARD
14.SYSTEM POWER(PVCORE&PVAXG-1)	39.SYSTEM MEMORY (DIMM1)	64.CRT DB WTB CONN
15.SYSTEM POWER(PVCORE&PVAXG-2)	40.EMPTY	65.MIC DB
16.POWER SEQUENCE (SLEEP)	41.EMPTY	66.SCREW
17.DC JACK & BATTERT CONN.	42.DP TO VGA CONVERTER	67.EMPTY
18.HP_OCP	43.DISPLAY PORT	68.MARS-1
19.PVCORE_DGPU	44.LCM & WEBCAM CONN	69.MARS-2
20.PVDDCI	45.SATA HDD, MSATA	70.MARS-3
21.P1V35S_DGPU	46.USB HUB	71.MARS-4
22.P1V8S	47.USB3 PORTS	72.MARS-5
23.PVPCIE	48.USB & CRT DB	73.MARS-6
24.POWER (SEQUENCE)	49.FINGERPRINT READER, NFC	74.MARS-7
25.FAN & THERMAL	50.ACCELEMETER	75.MARS-8
		76.VRAM-1
		77.VRAM-2

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
TABLE OF CONTENTS			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 3 of 77			





LATCHED_ALARM OUT

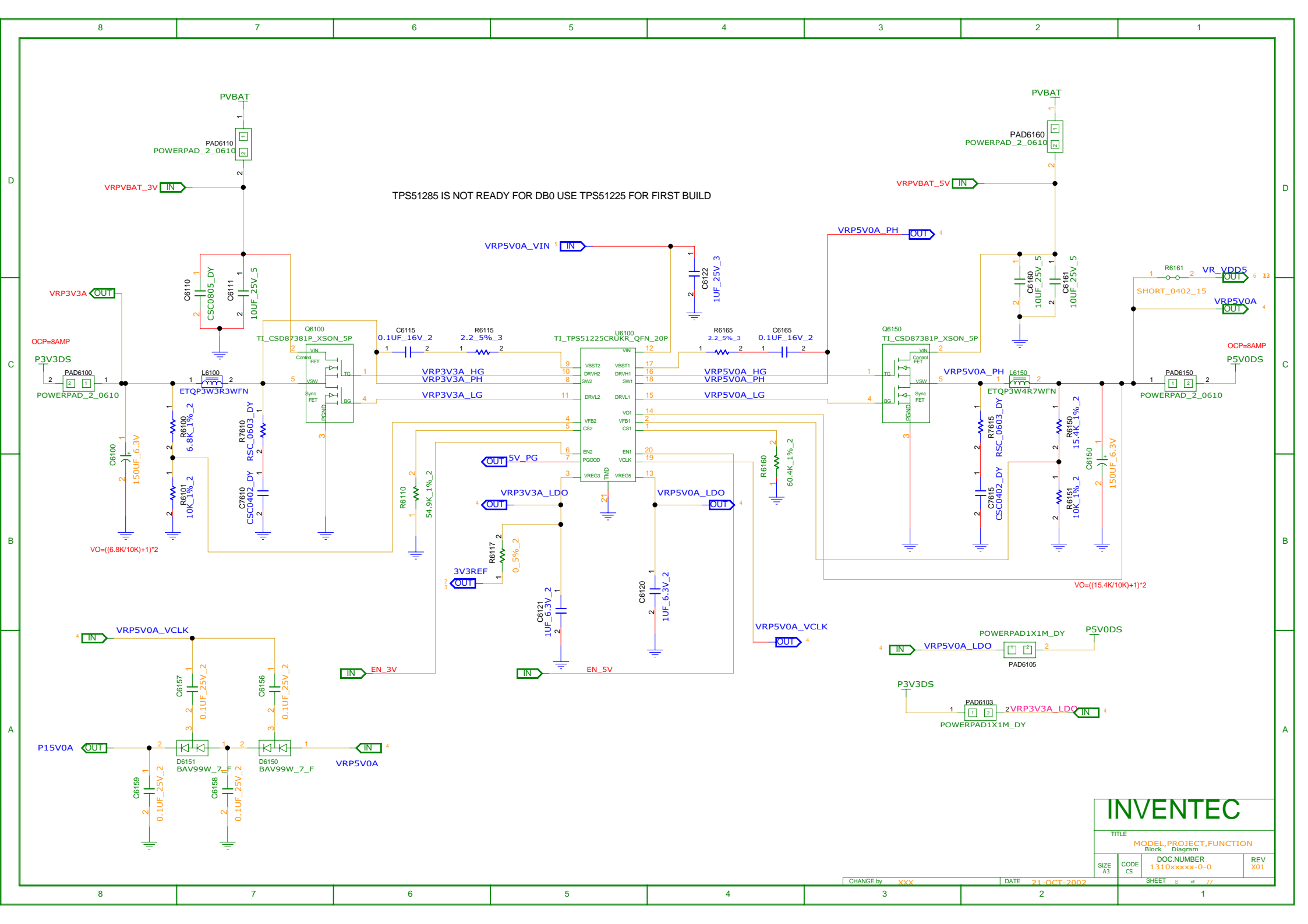
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 6 of 77



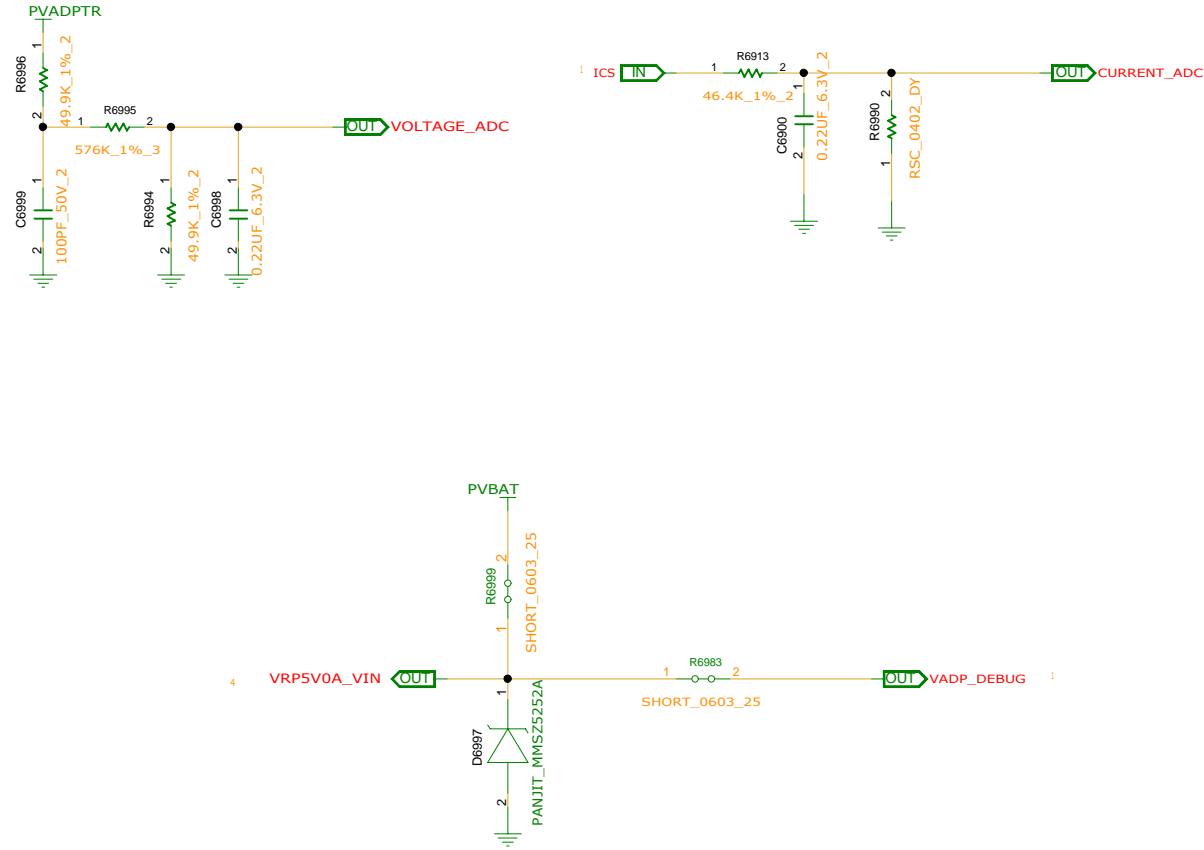
TPS51285 IS NOT READY FOR DB0 USE TPS51225 FOR FIRST BUILD

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 8 of 77

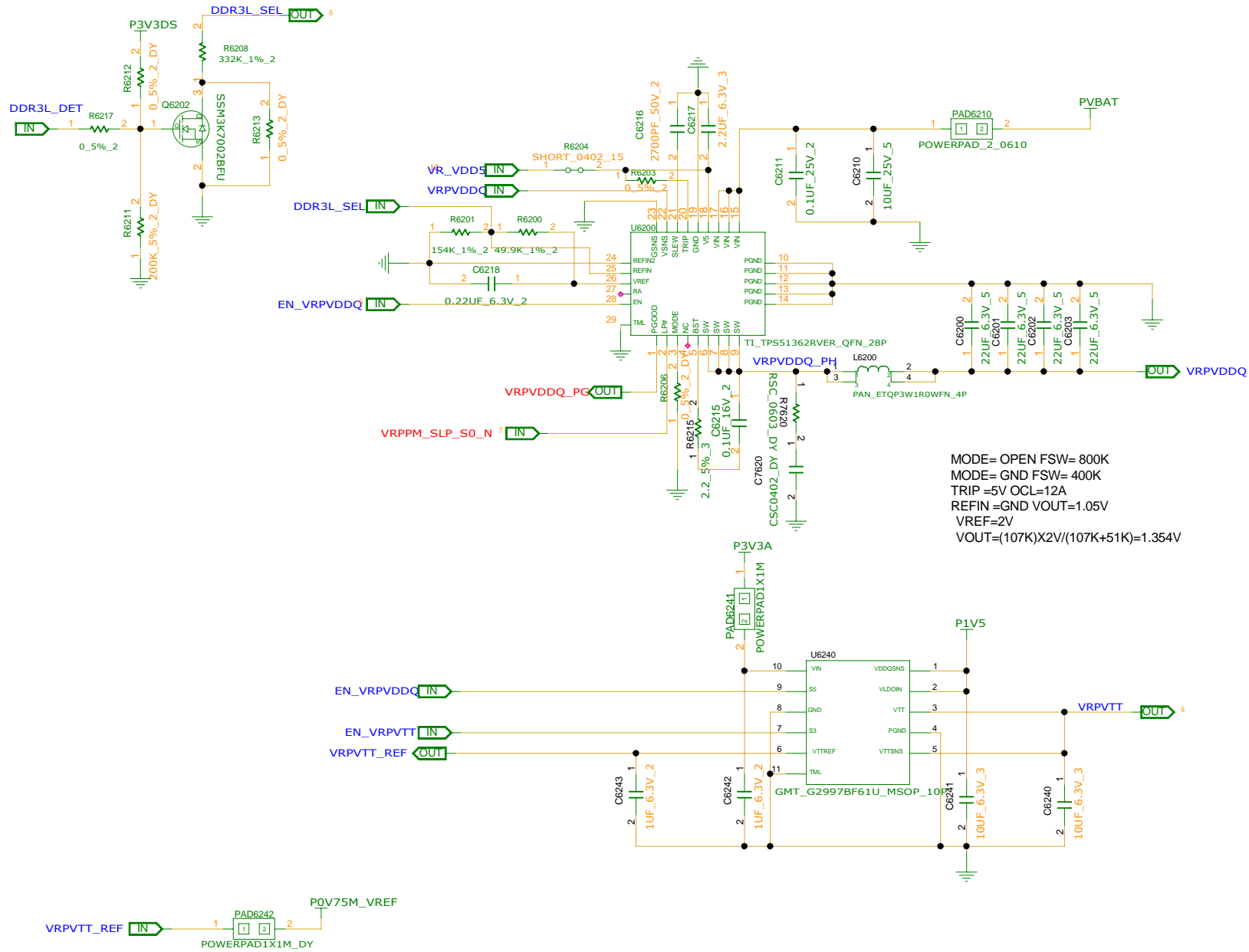


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

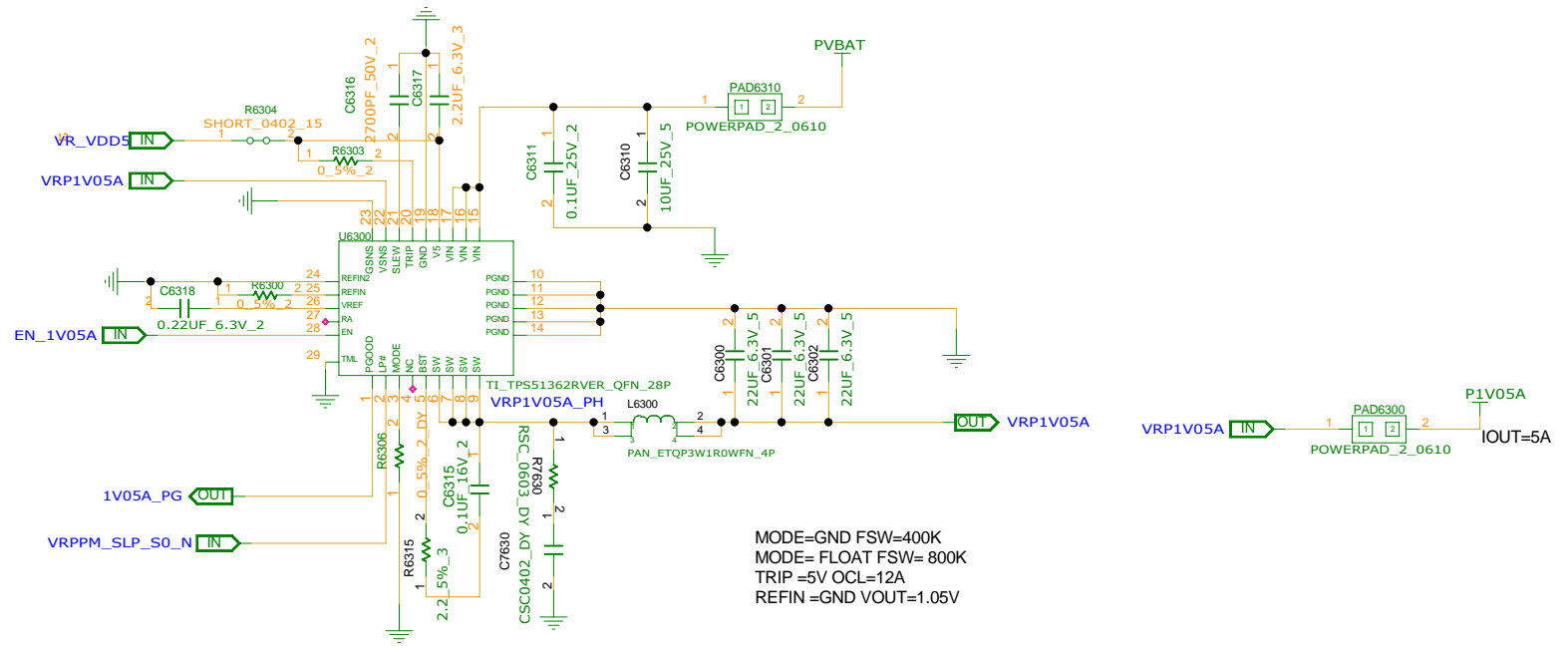
SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

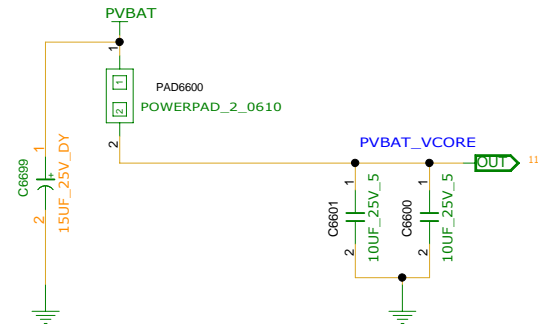
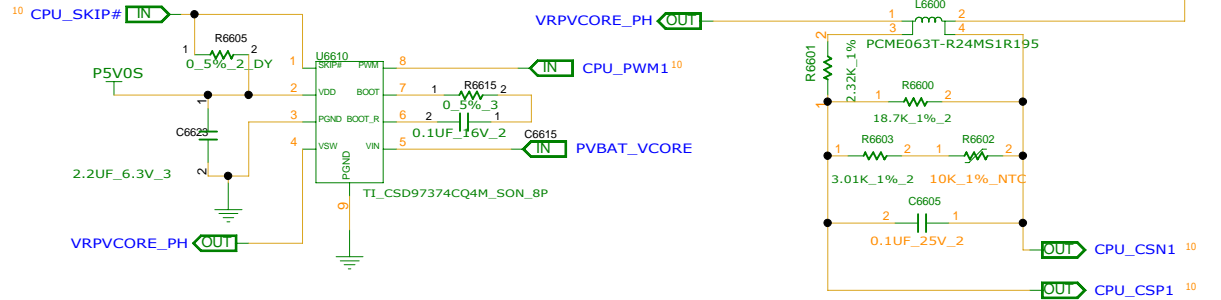
CHANGE by XXX DATE 21-OCT-2002 SHEET 8 of 77



MODE= OPEN FSW= 800K
 MODE= GND FSW= 400K
 TRIP =5V OCL=12A
 REFIN =GND VOUT=1.05V
 VREF=2V
 $VOUT=(107K) \times 2V / (107K + 51K) = 1.354V$

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION			
DOC NUMBER 1310xxxxx-0-0			
SIZE A3	CODE CS	REV X01	
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 10 of 77			





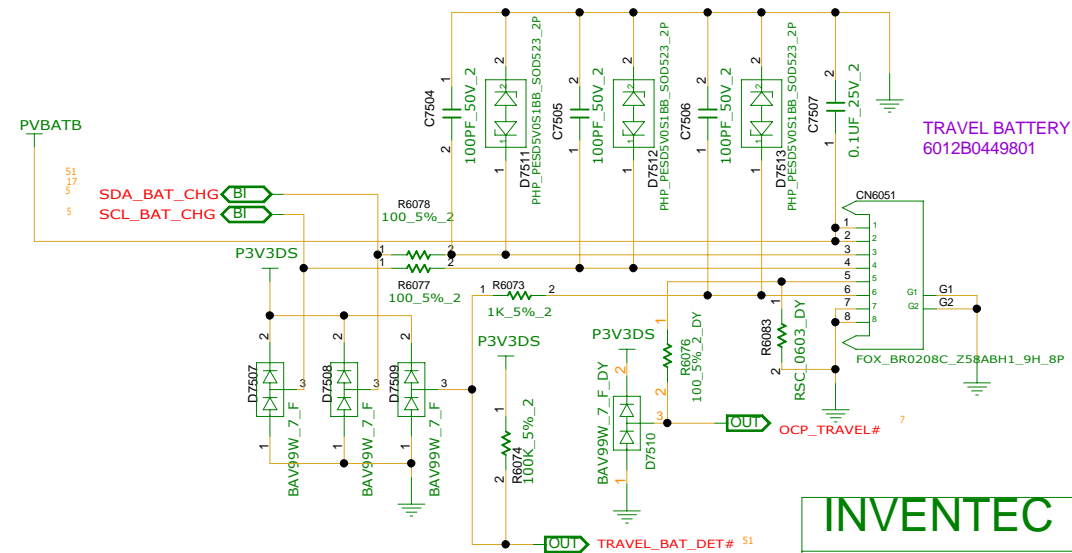
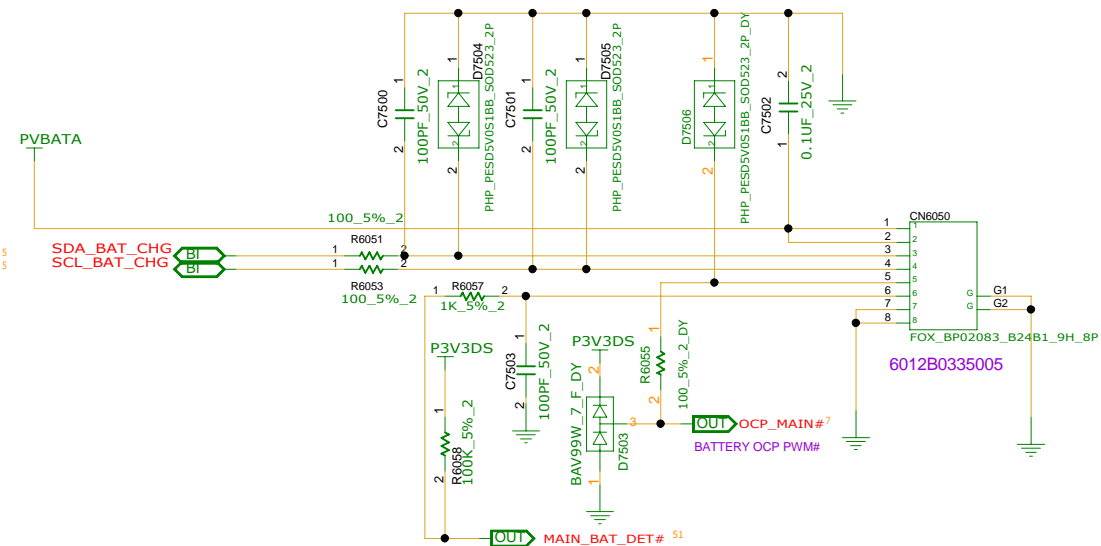
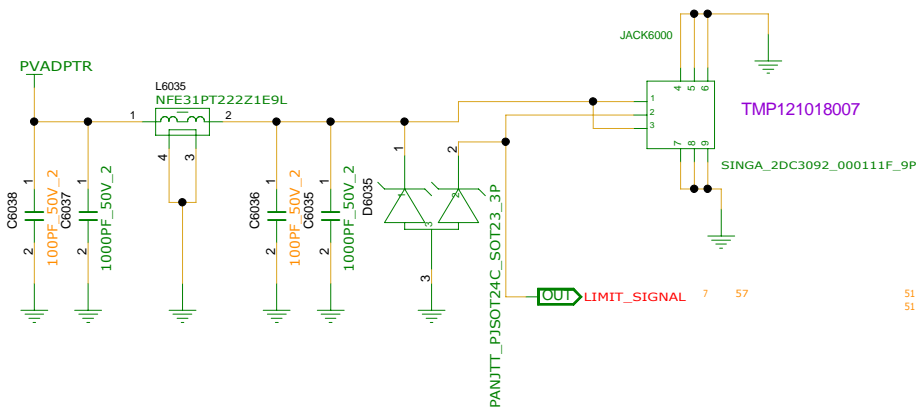
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

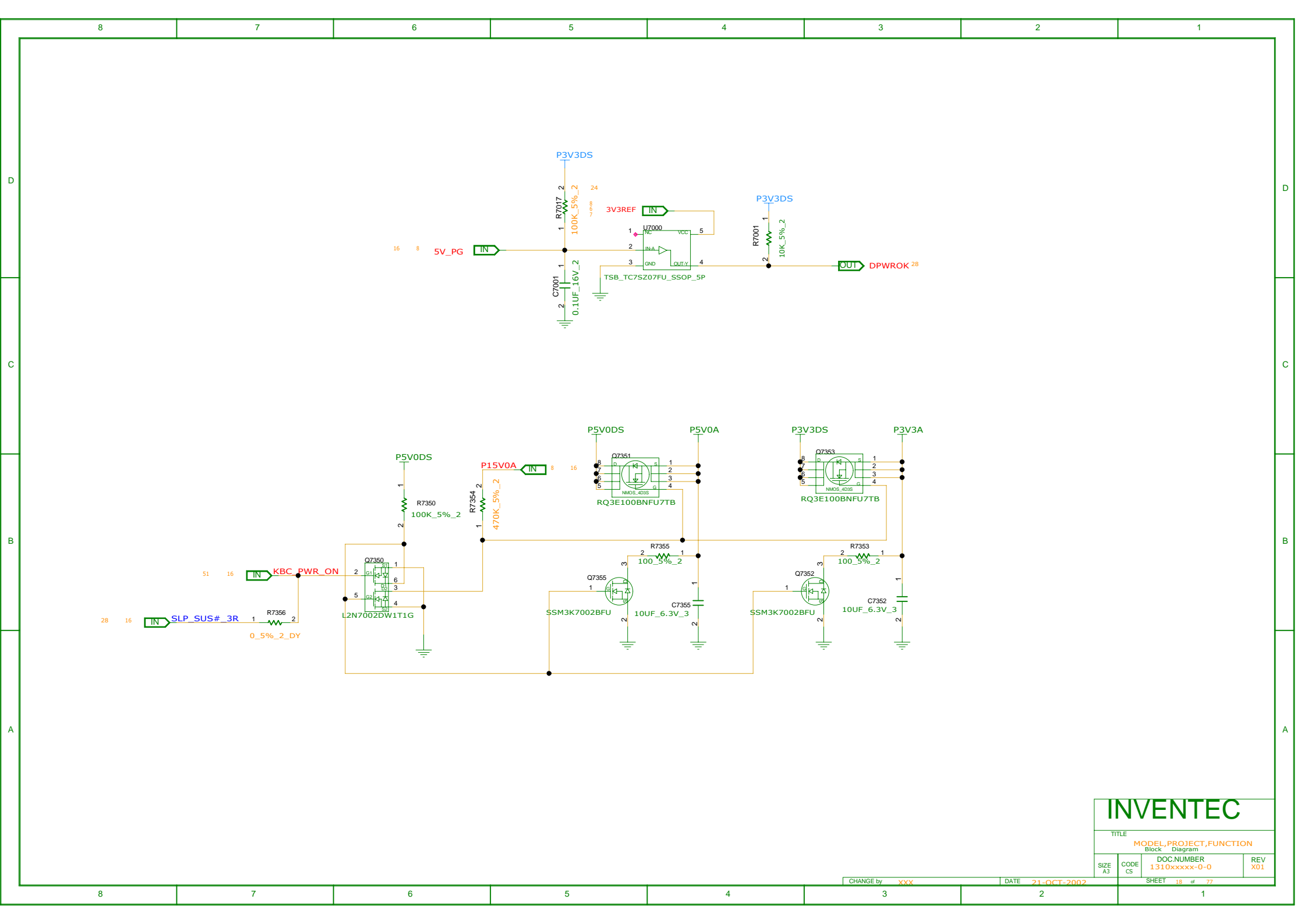
[illegible]

TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
DOC NUMBER		REV	
1310xxxxx-0-0		X01	
SIZE	CODE	SHEET	
A3	CS	17 of 77	

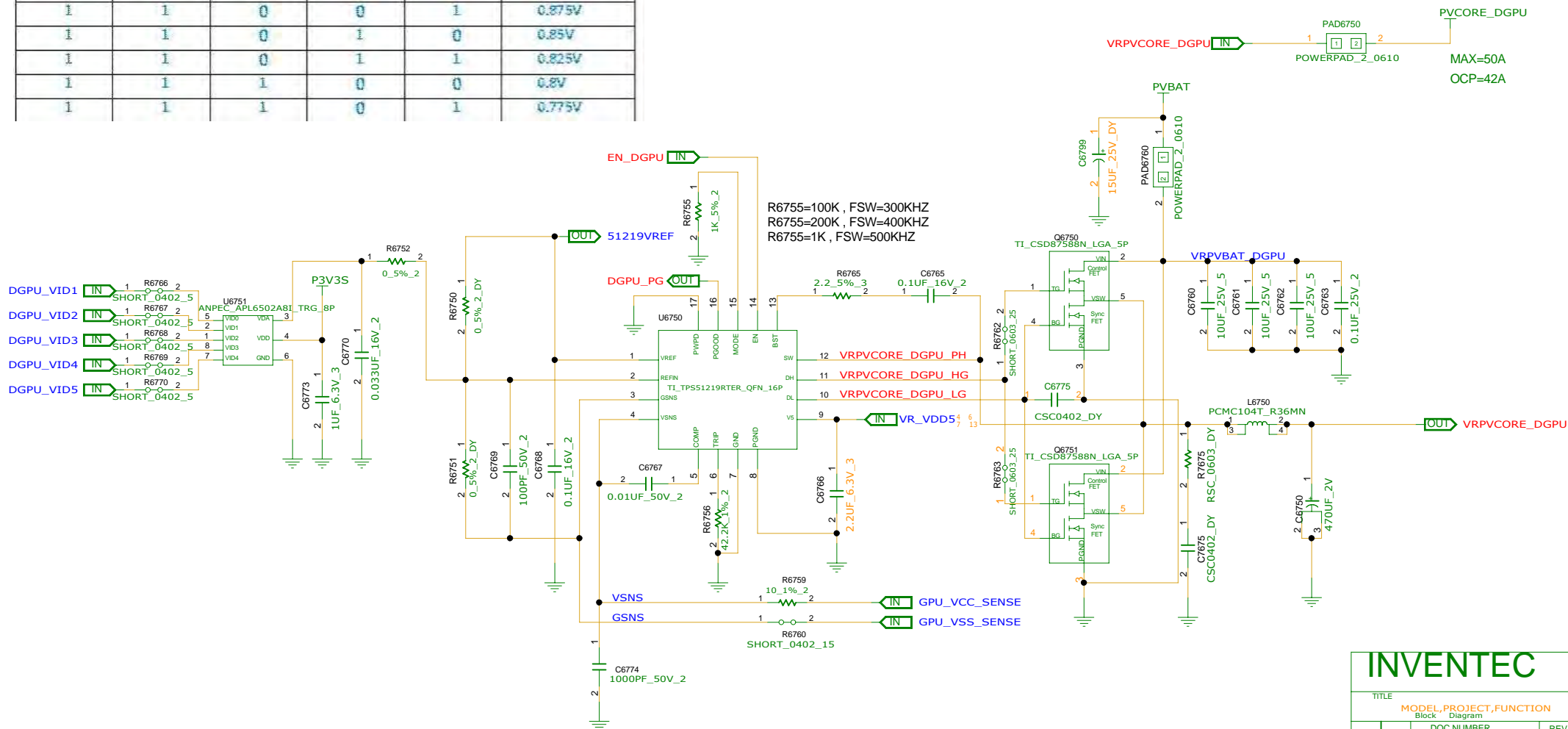


INVENTEC

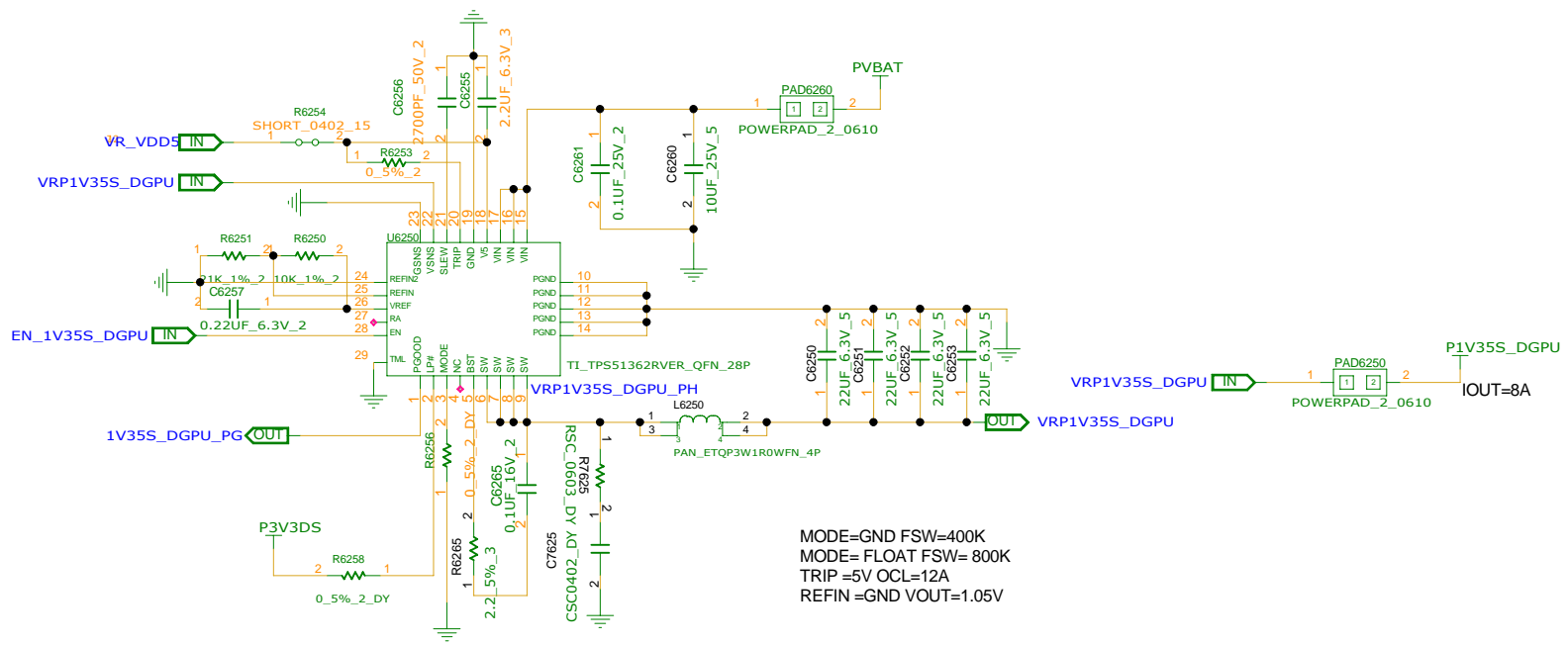
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

GPU_VID5 GPIO_10	GPU_VID4 GPIO_14	GPU_VID3 GPIO_15	GPU_VID2 GPIO_16	GPU_VID1 GPIO_20	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1.0V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

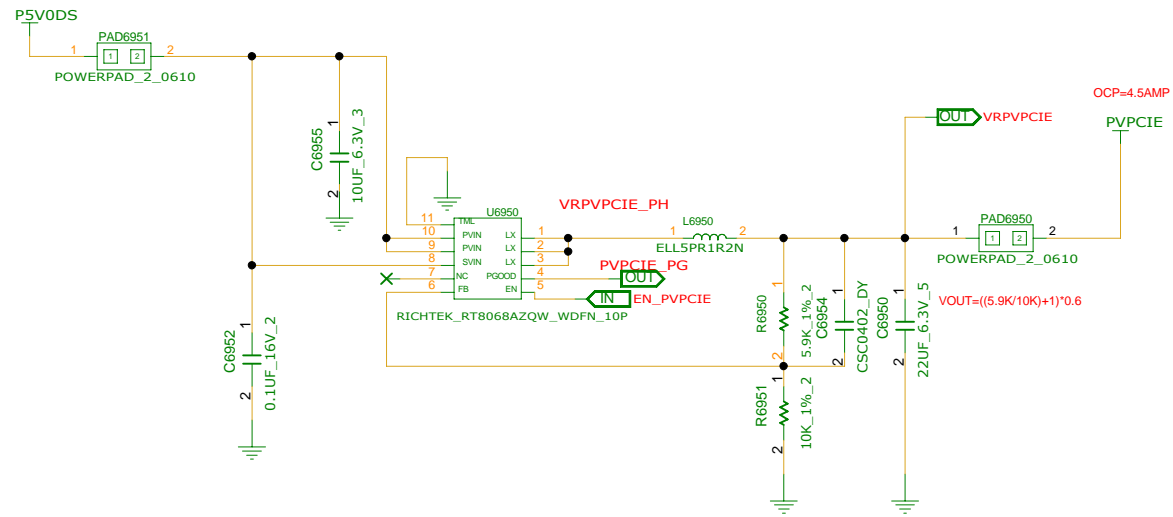
	C6762	C6752	L6750	Q6751	R6756
17W	OPEN	OPEN	ETQP4LR36AFM 6014B0164501	OPEN	80.6K_1% 6013A0072901
25W	install	install	PCMC104T-R36MN 6014B0024003	install	42.2K_1% 6013A0017701



EMPTY



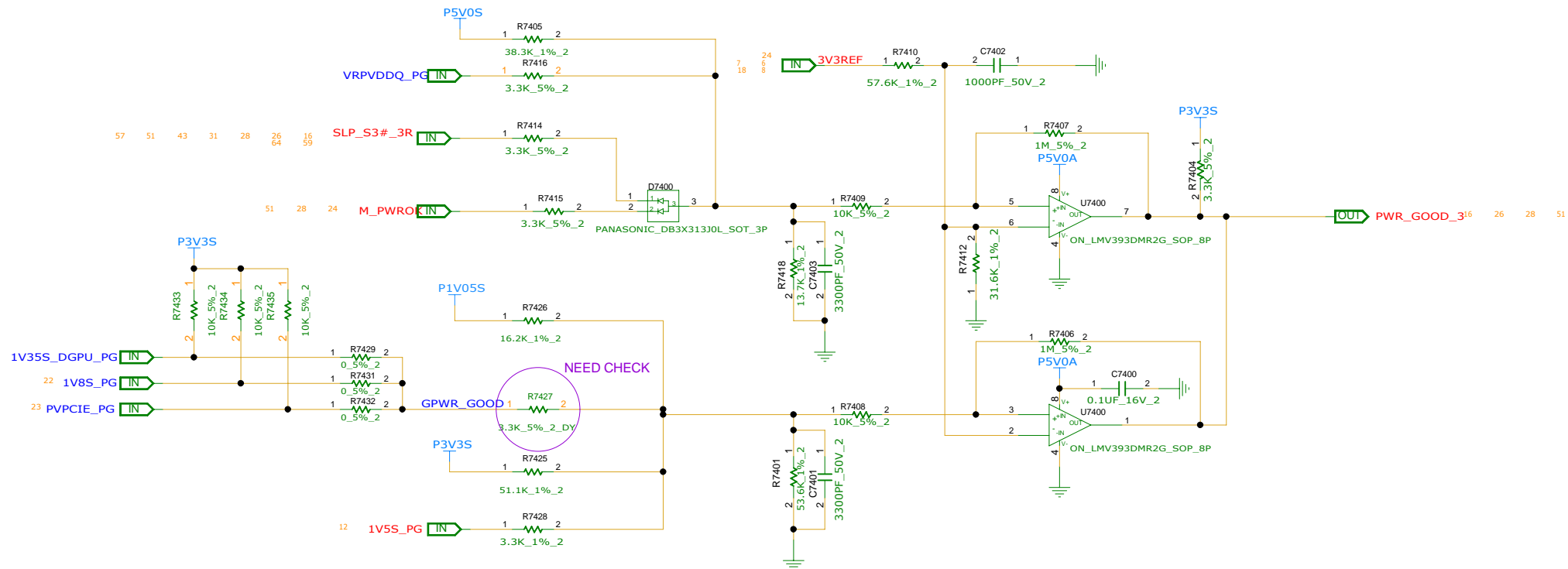
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXXX			
DATE 21-OCT-2002			
SHEET 21 of 77			



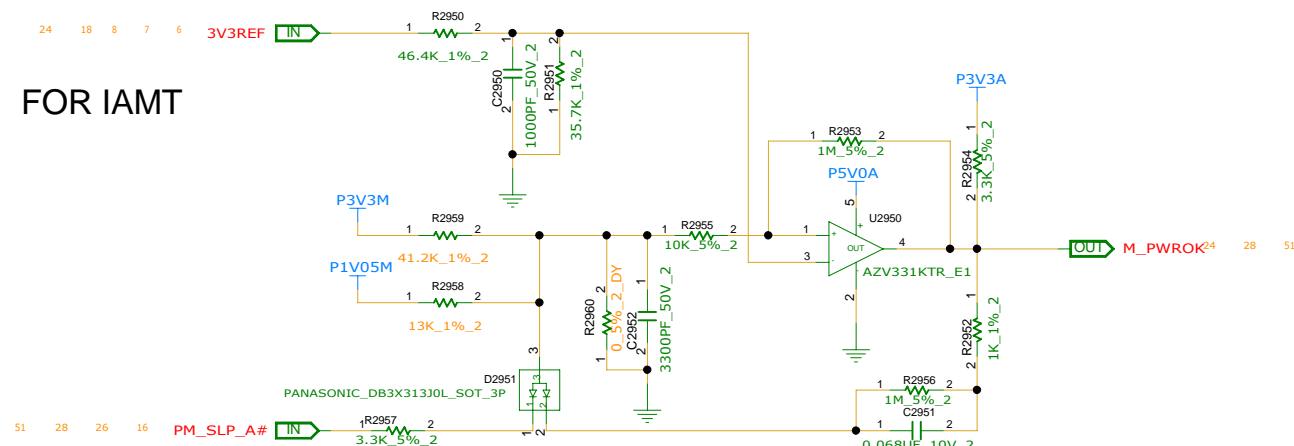
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

REFERENCE NUMER : 7400~7450



FOR IAMT



REFERENCE NUMER : 2950~2999

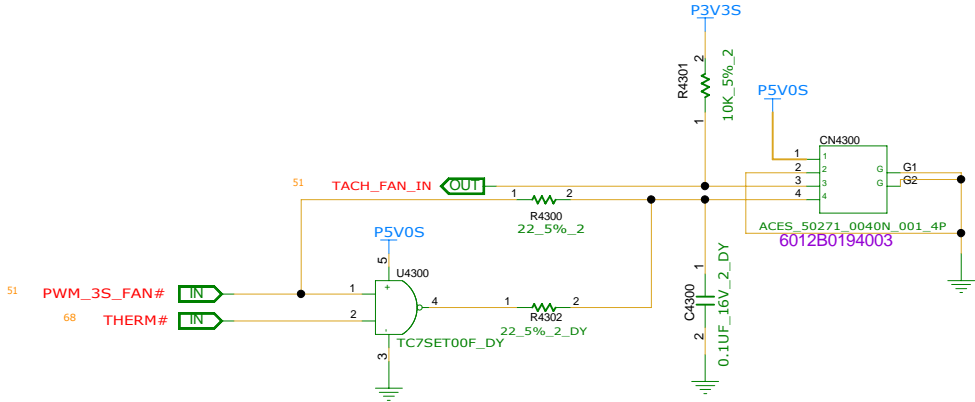
INVENTEC

TITLE			
MODEL PROJECT FUNCTION POWER (SEQUENCE)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01

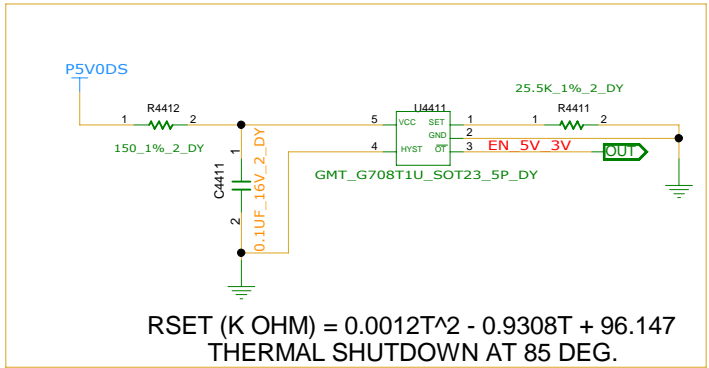
CHANGE by XXX DATE 21-OCT-2002

SHEET 24 of 77

REFERENCE NUMBER:4400~4349



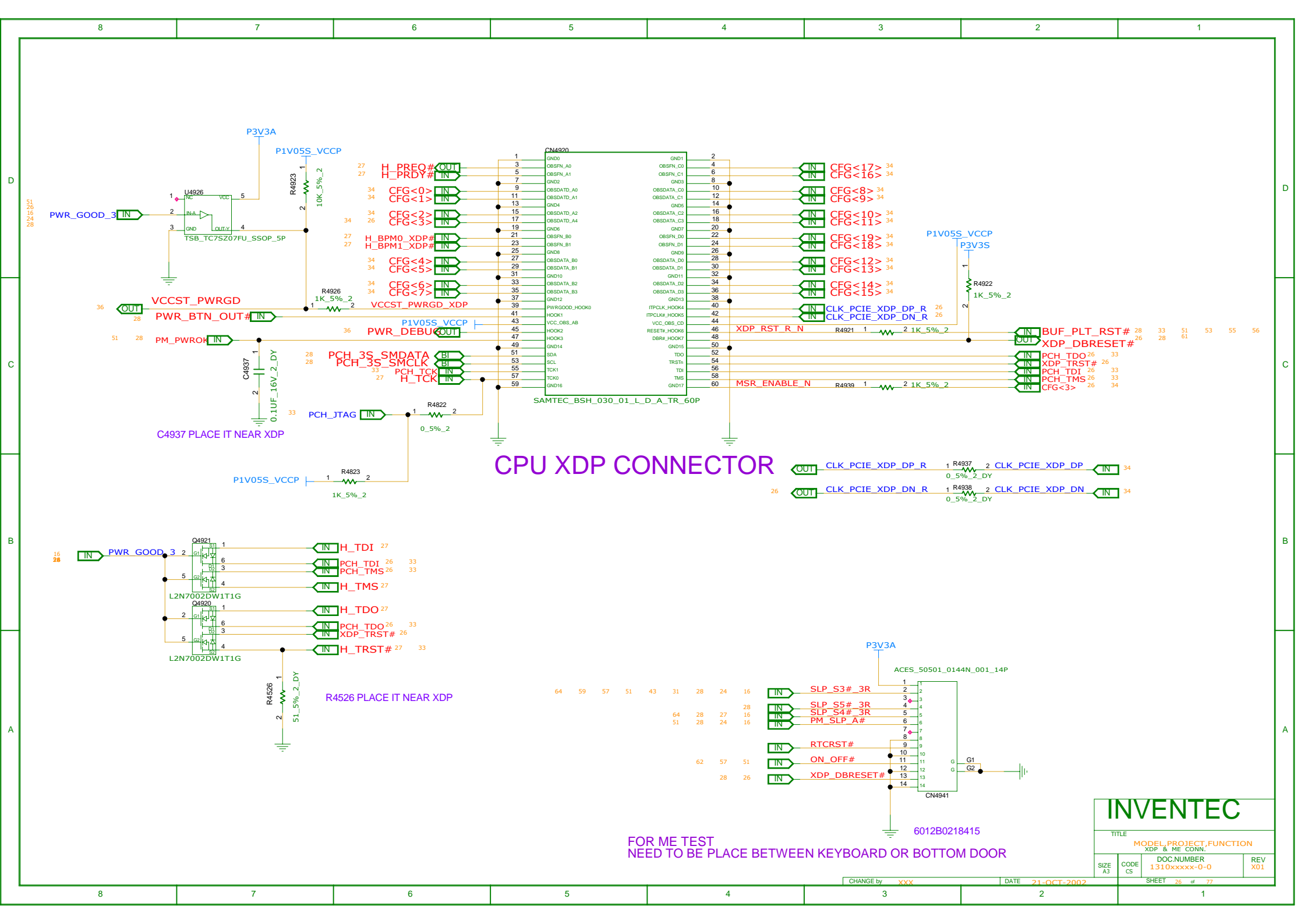
AMBIENT TEMP SENSE
WILL BE NOT USED IN 2013?

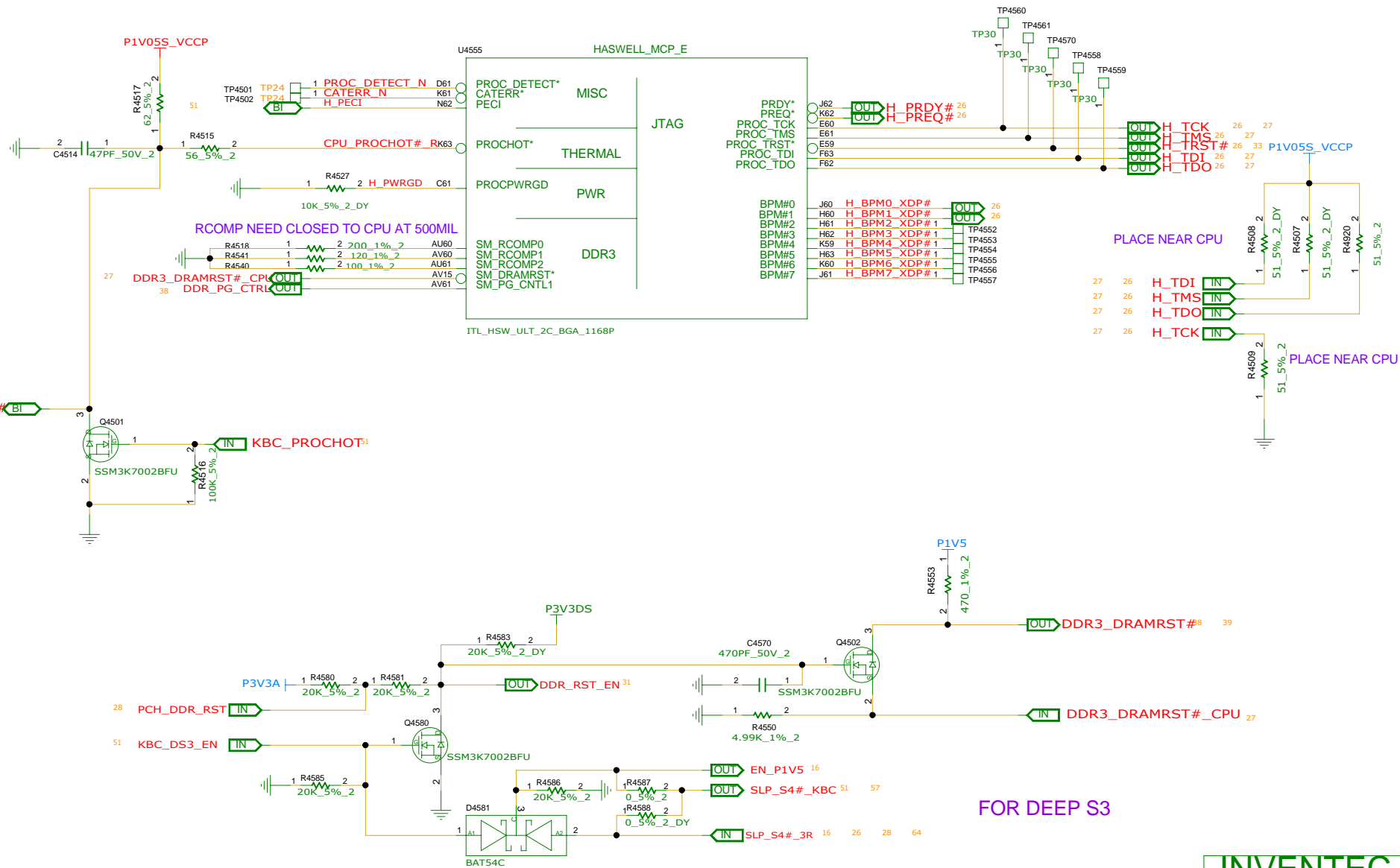


REFERENCE NUMBER:4411~4449

INVENTEC

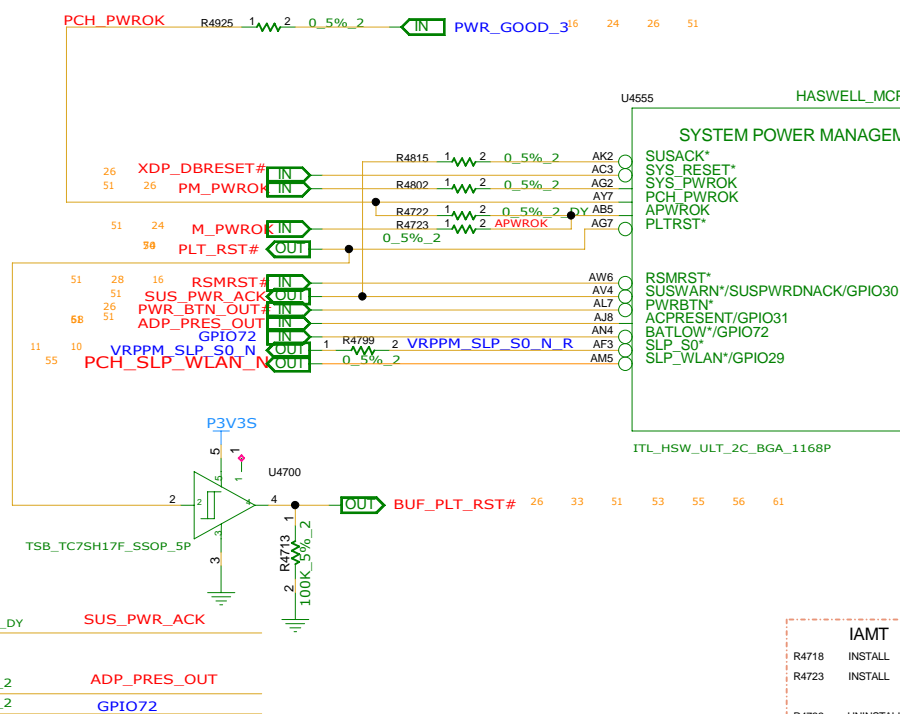
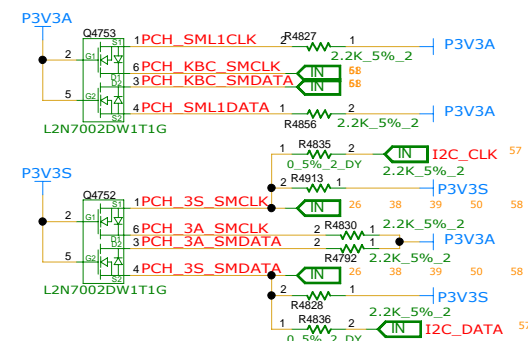
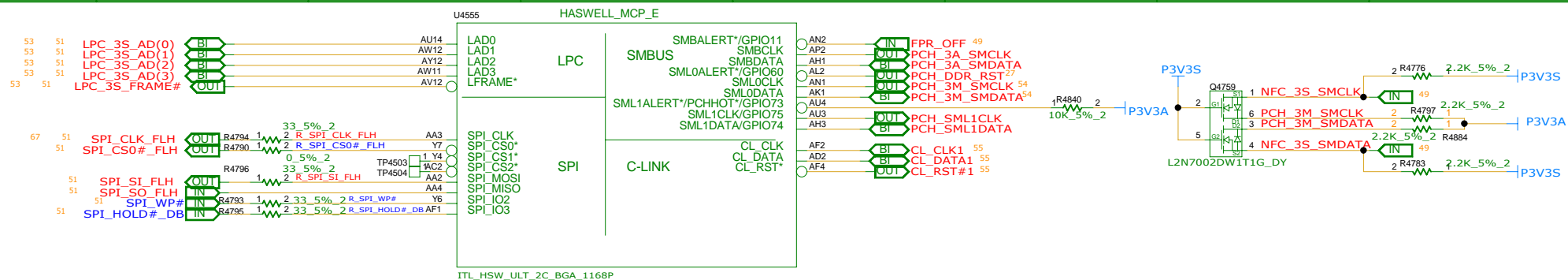
TITLE			
MODEL PROJECT,FUNCTION			
FAN & THERMAL			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01





REFERENCE:4500~4949

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
MCP1-MISC			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	27 of 77



	IAMT	NON-IAMT
R4718	INSTALL	UNINSTALL
R4723	INSTALL	UNINSTALL
R4722	UNINSTALL	INSTALL

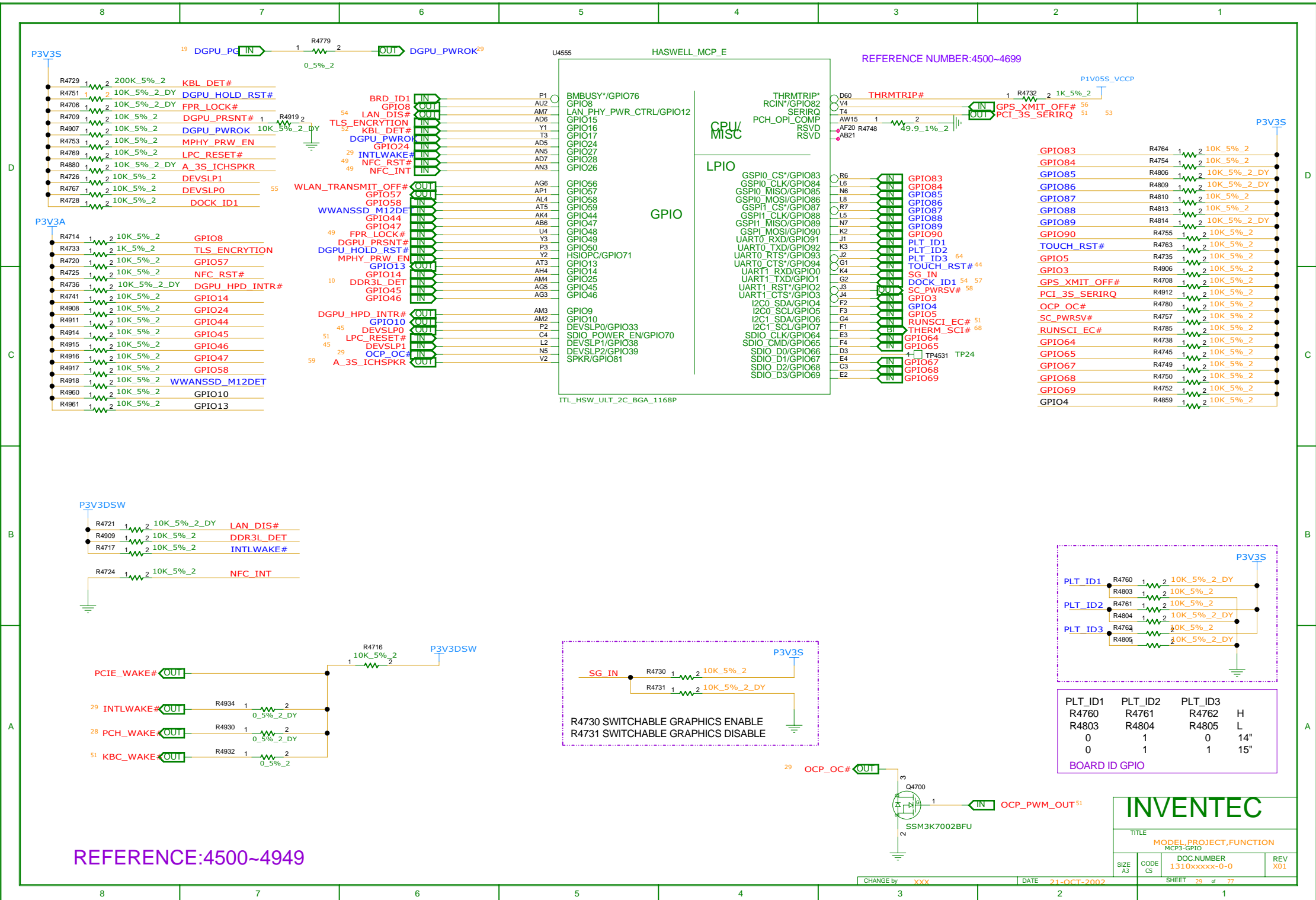
REFERENCE:4500~4949

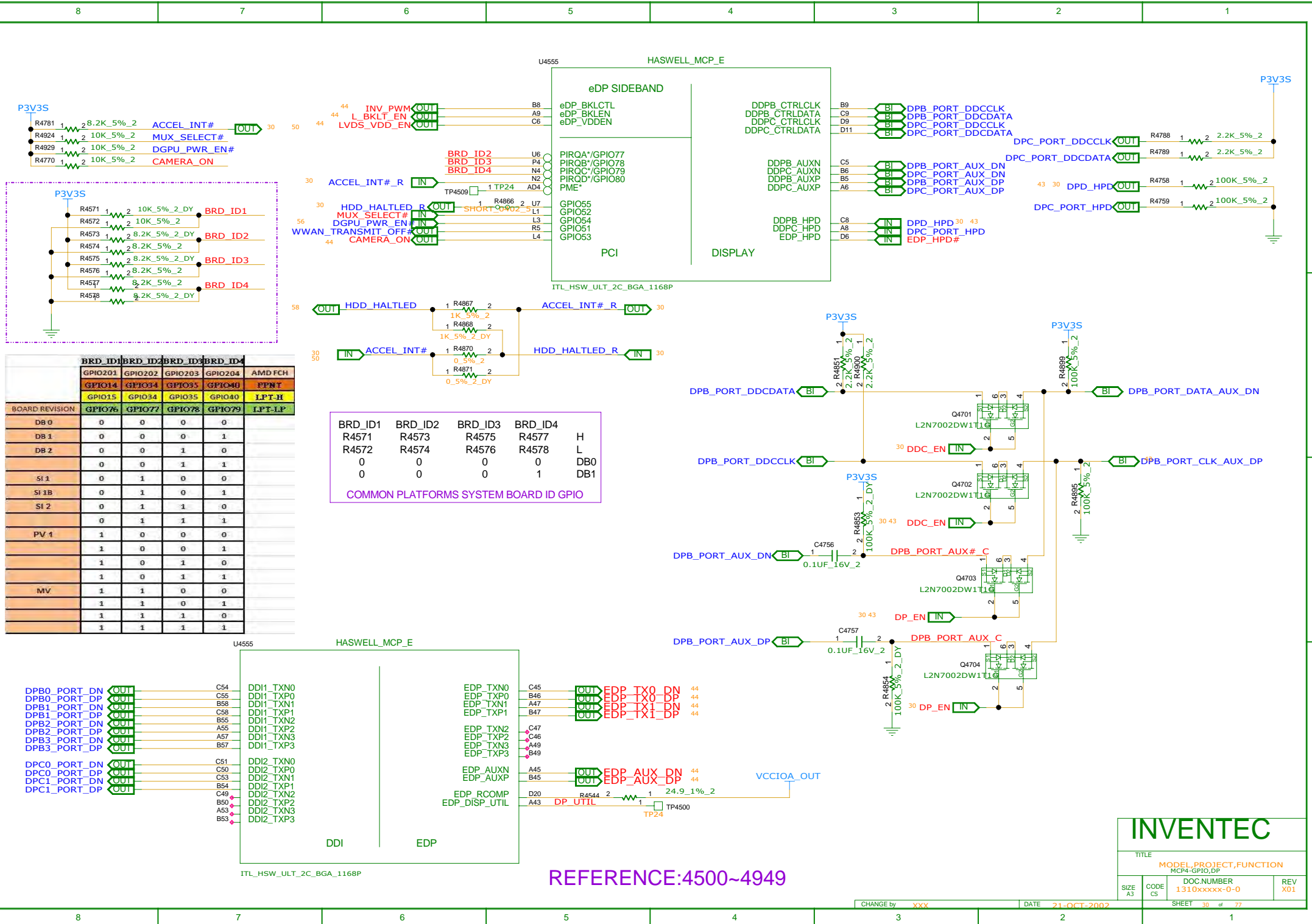
INVENTEC

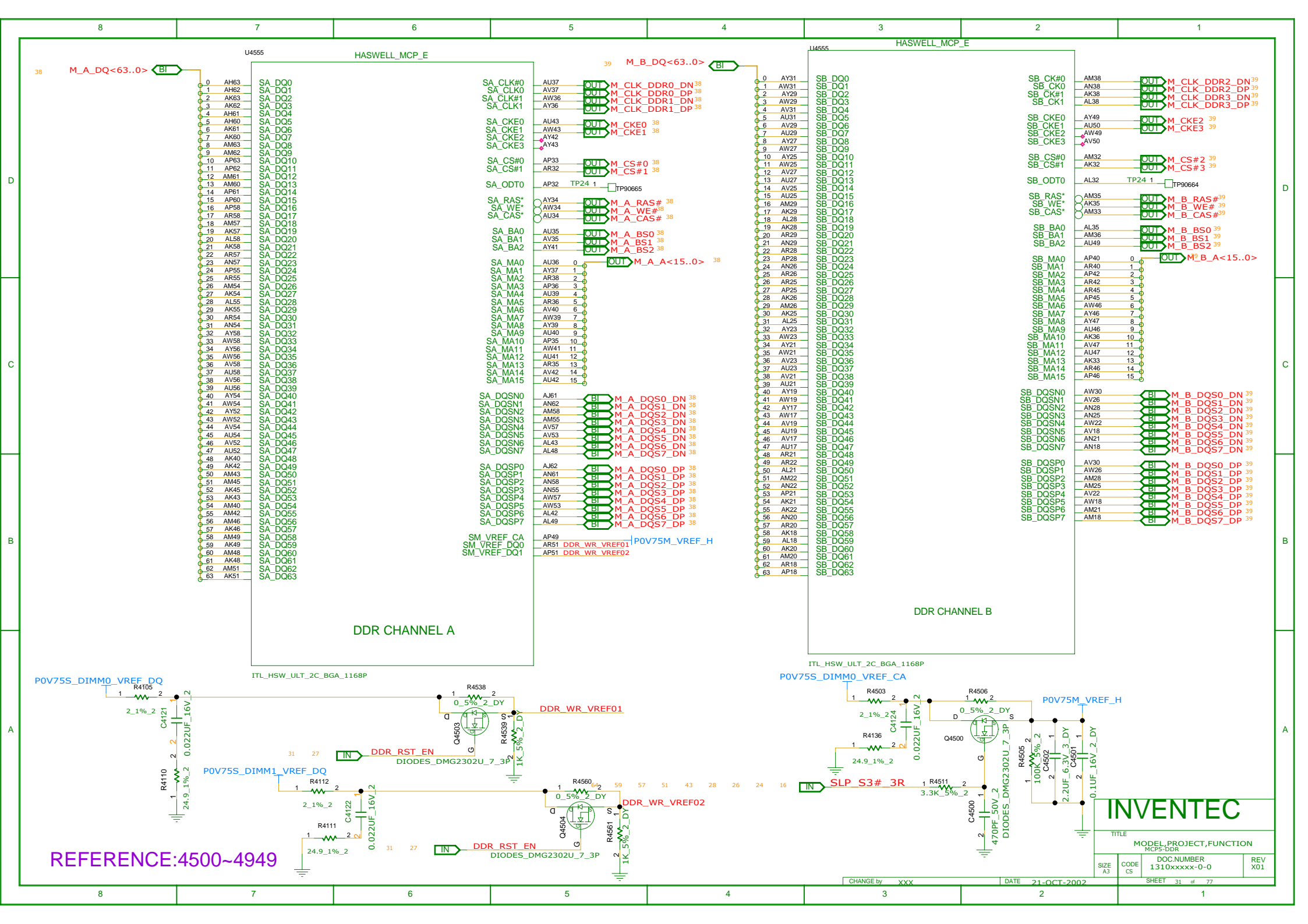
TITLE			
MODEL,PROJECT,FUNCTION			
MCP2-SPI,SMBUS,SYSTEM		SRQUENCE	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 28 of 77			

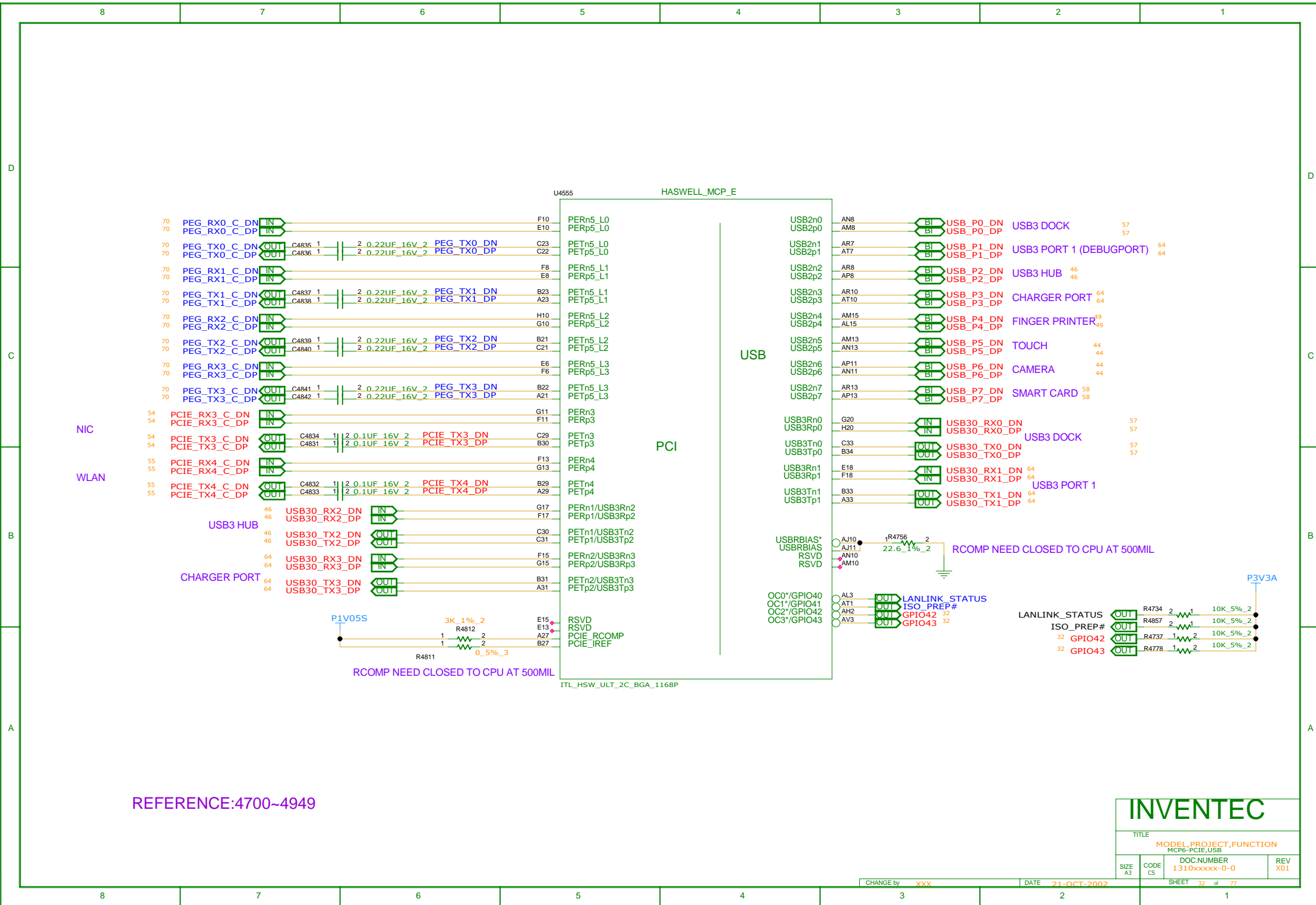
CHANGE by	XXX	DATE	21-OCT-2002
-----------	-----	------	-------------

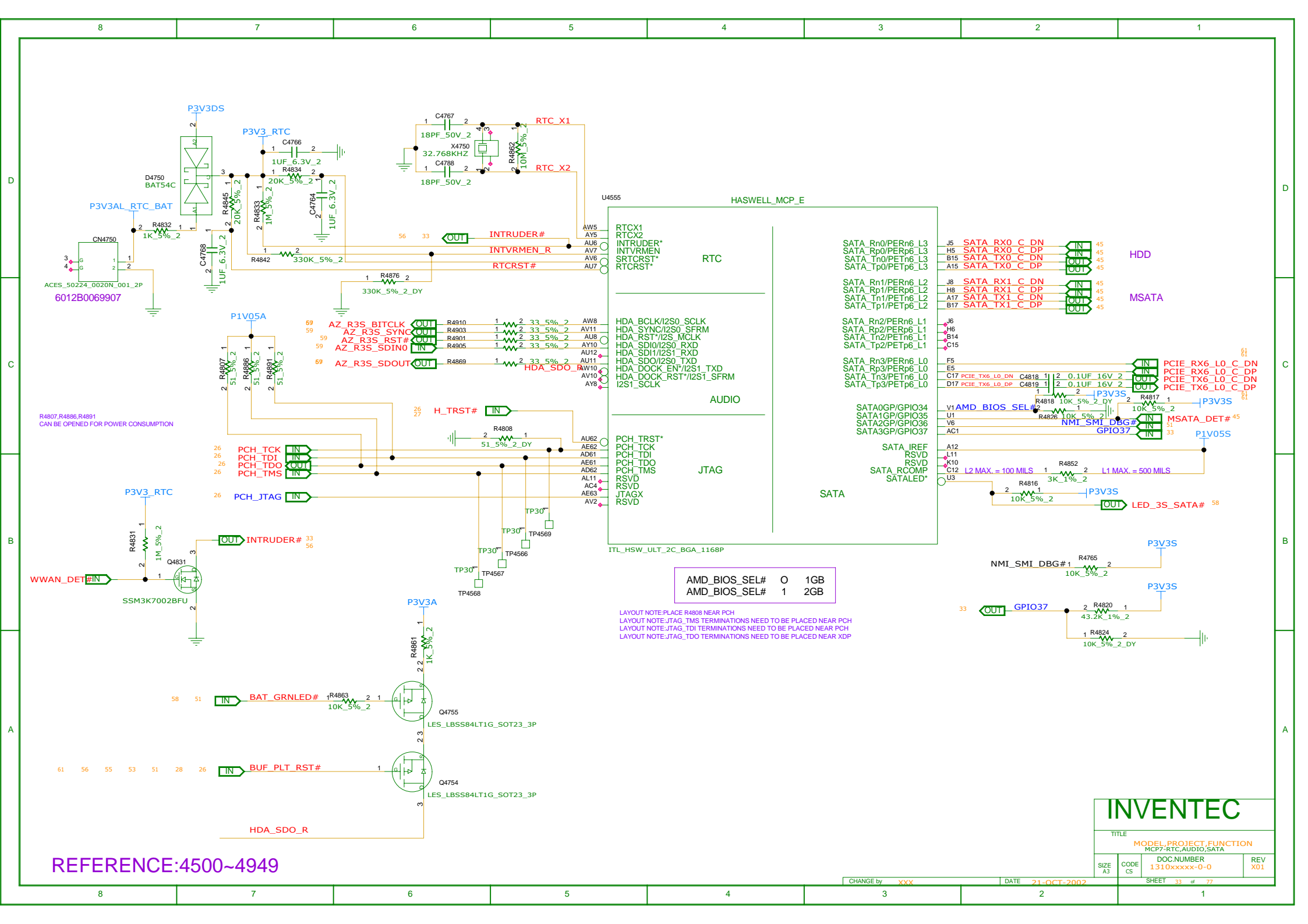
SHEET 28 of 77



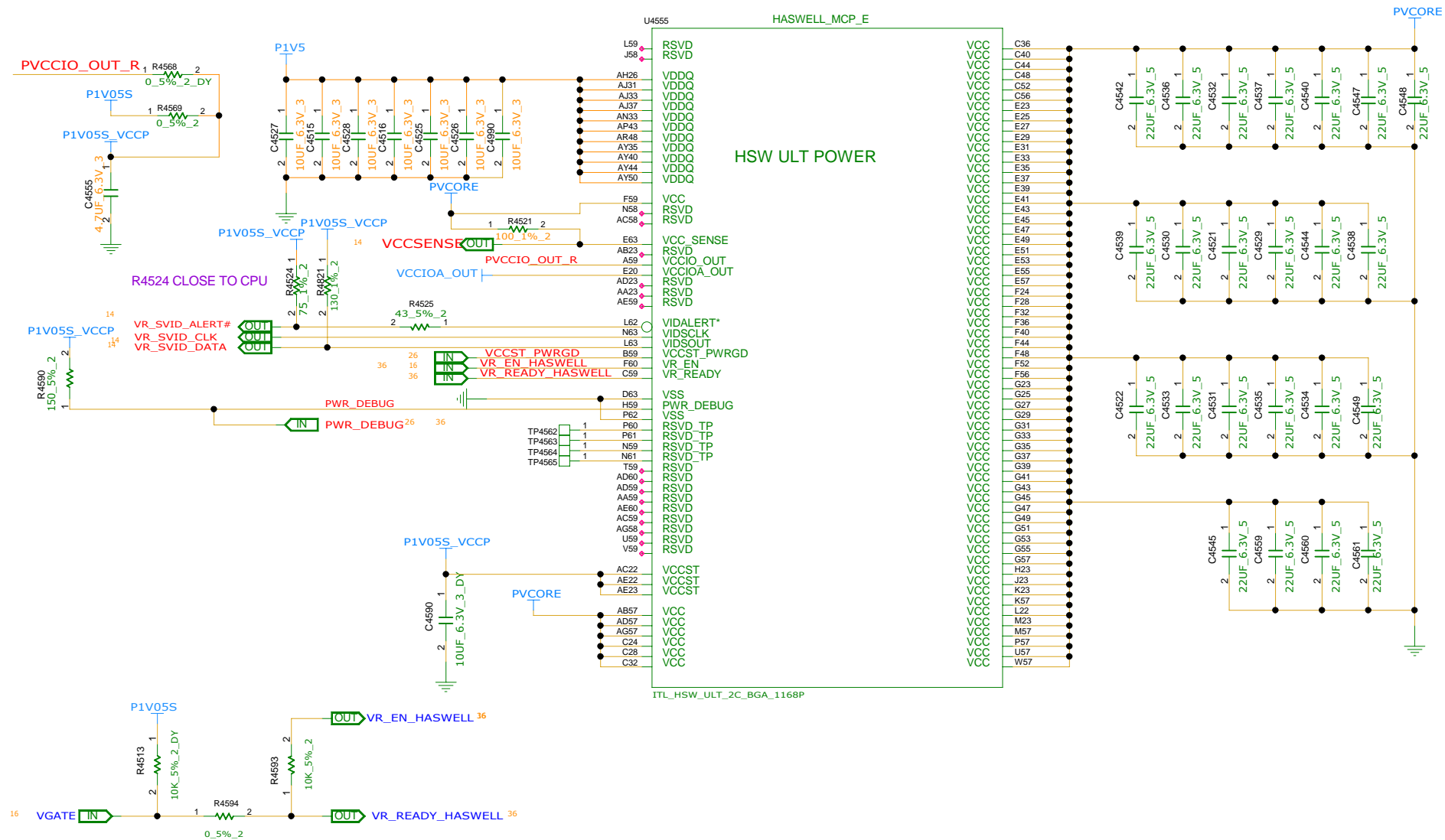








ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



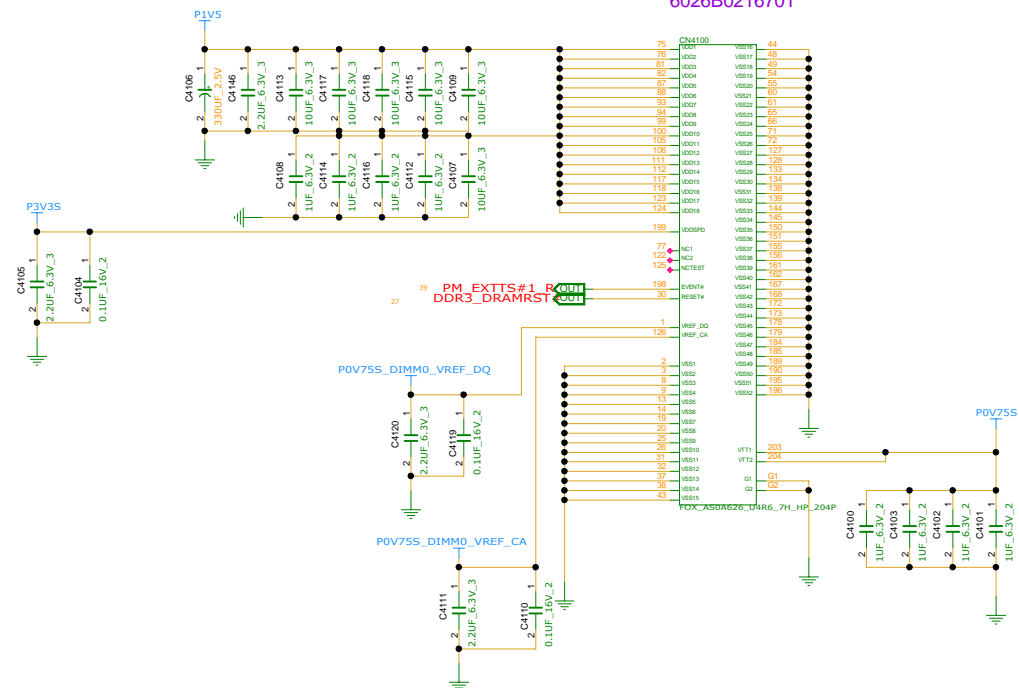
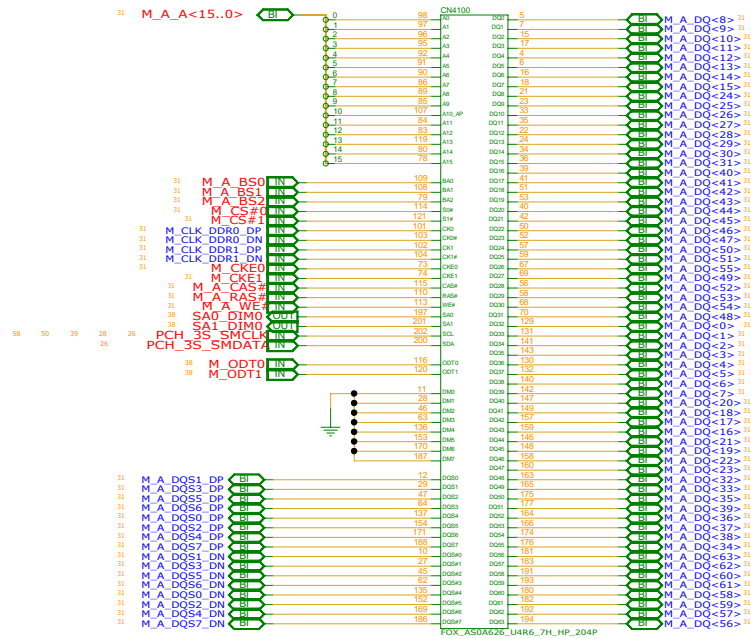
REFERENCE:4500~4949

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION MCP10-POWER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 36 of 77			



SHEET 37 of 7

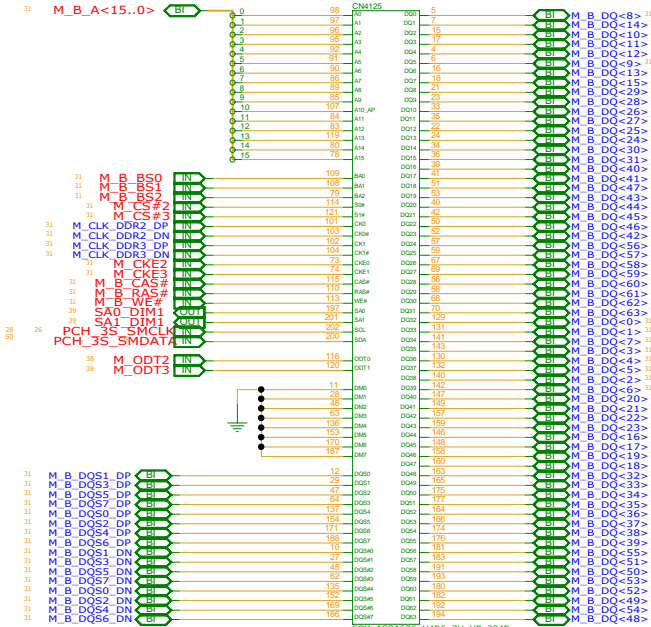
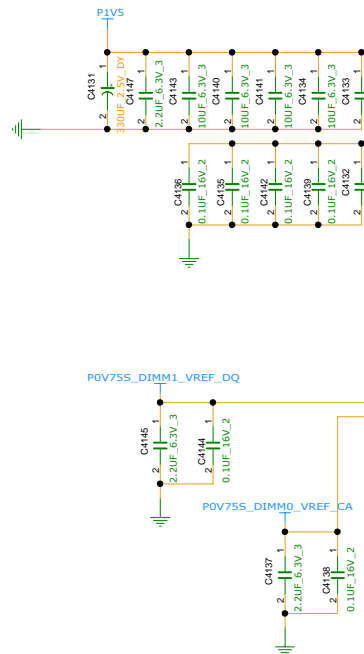
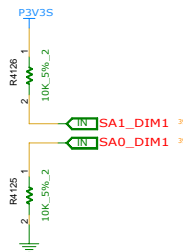
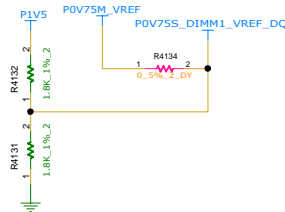


INVENTEC

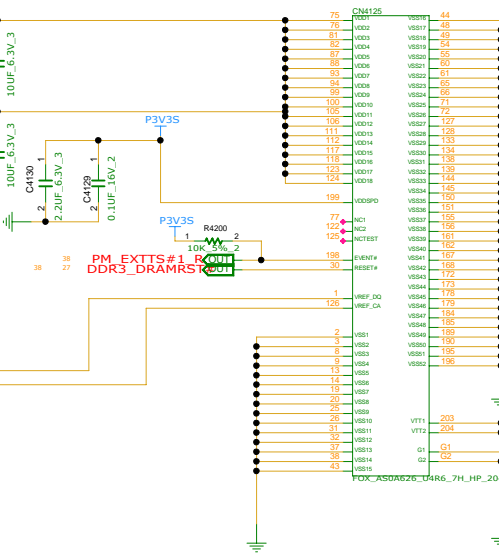
TITLE			
MODEL,PROJECT,FUNCTION DDR3_SO-DIMMO			
SIZE C	CODE CS	DOC NUMBER 1310xxxxxx-0-0	REV X01

NOTE:
SO-DIMM SPD ADDRESS IS 0X44
SO-DIMM TS ADDRESS IS 0X34

REFERENCE NUMBER:4100~4299



6026B0216701



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
DDR3_SO-DIMM0			
SIZE	CODE	DOC NUMBER	REV
C	CS	13100XXXX-0-0	201
SHEET			
38 of 37			

CHANGE BY: xxx DATE: 21-OCT-2002

RESERVED

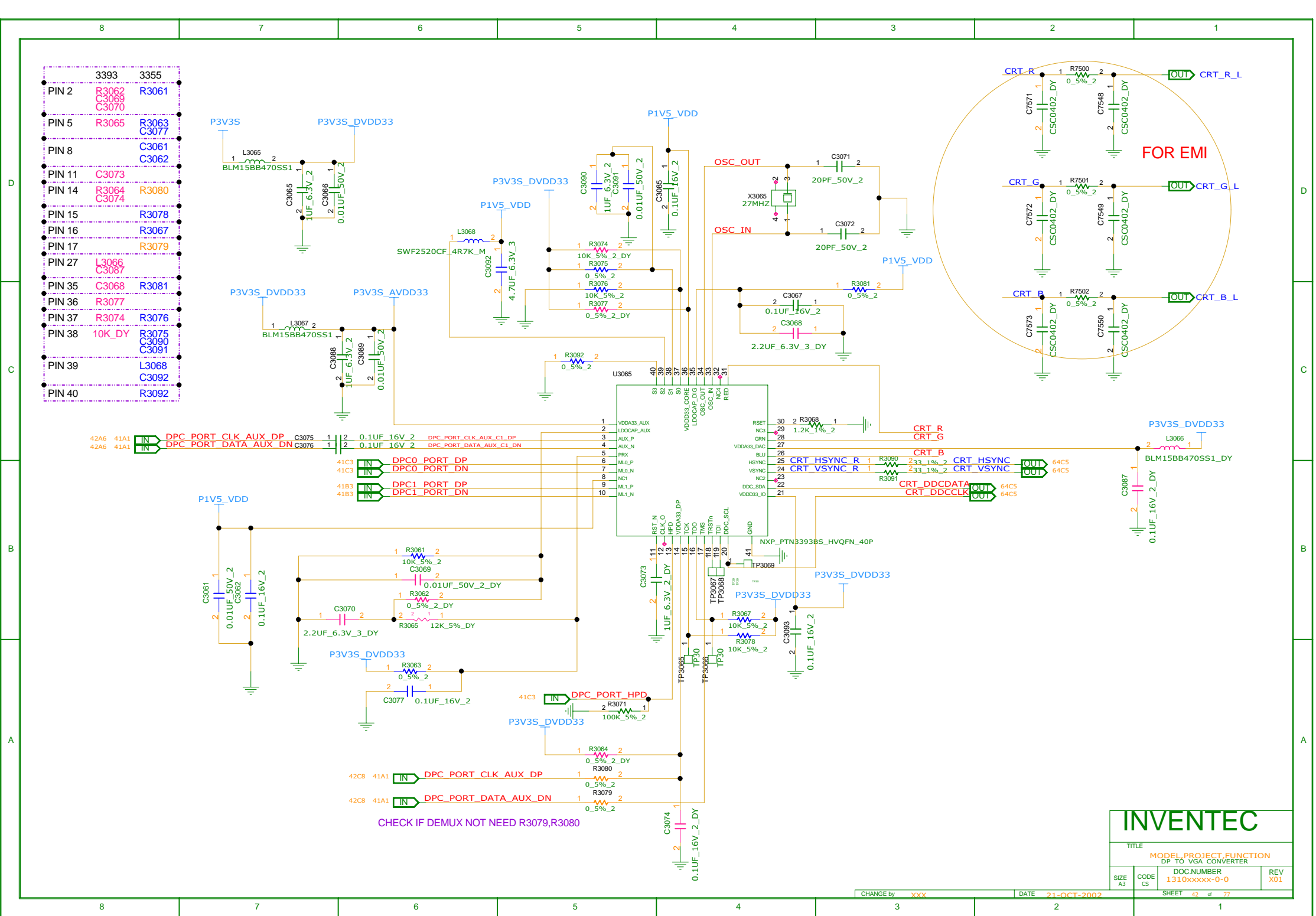
INVENTEC

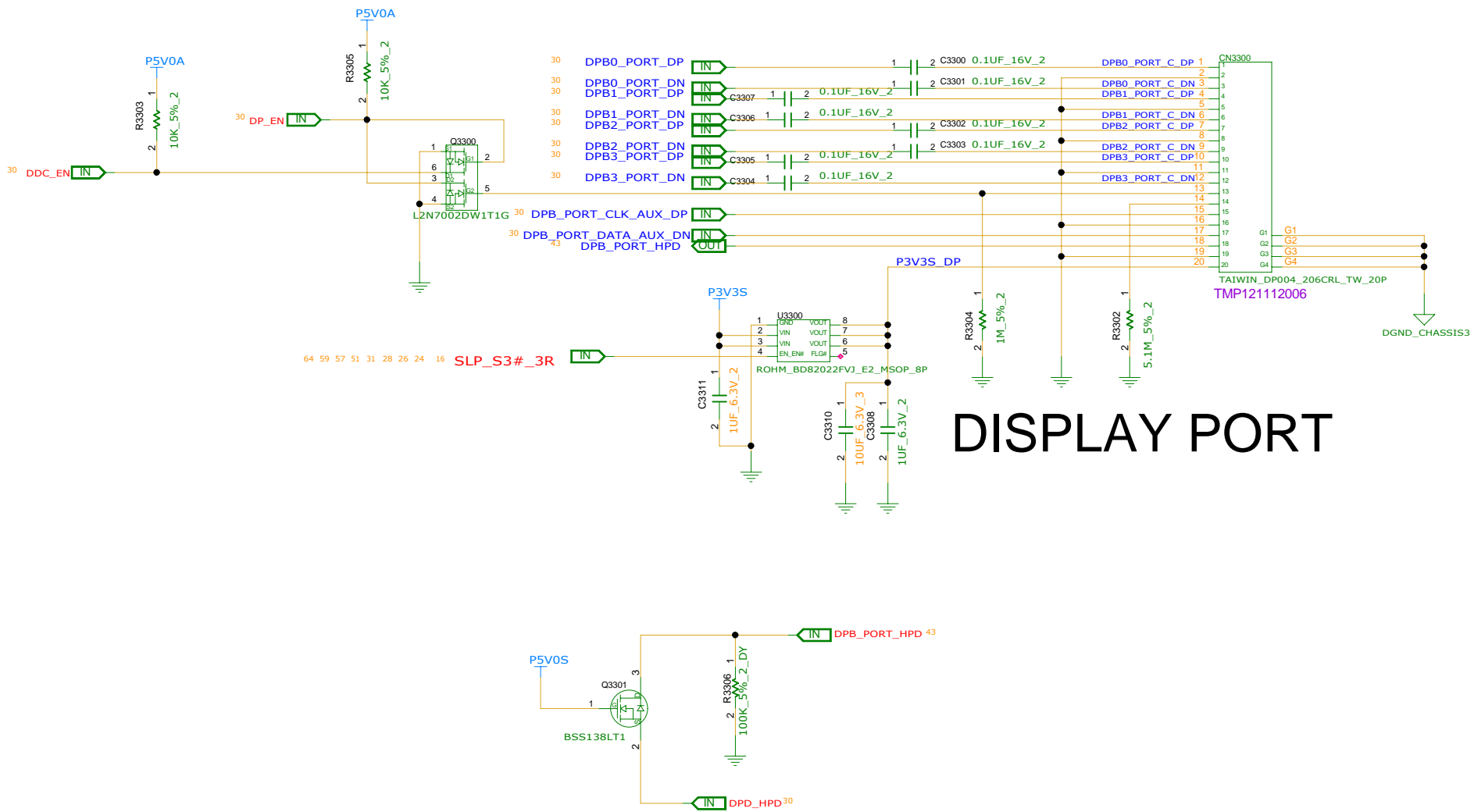
TITLE			
MODEL PROJECT FUNCTION DPB DEMUX1 TO DP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 40 of 77			

RESERVED

INVENTEC

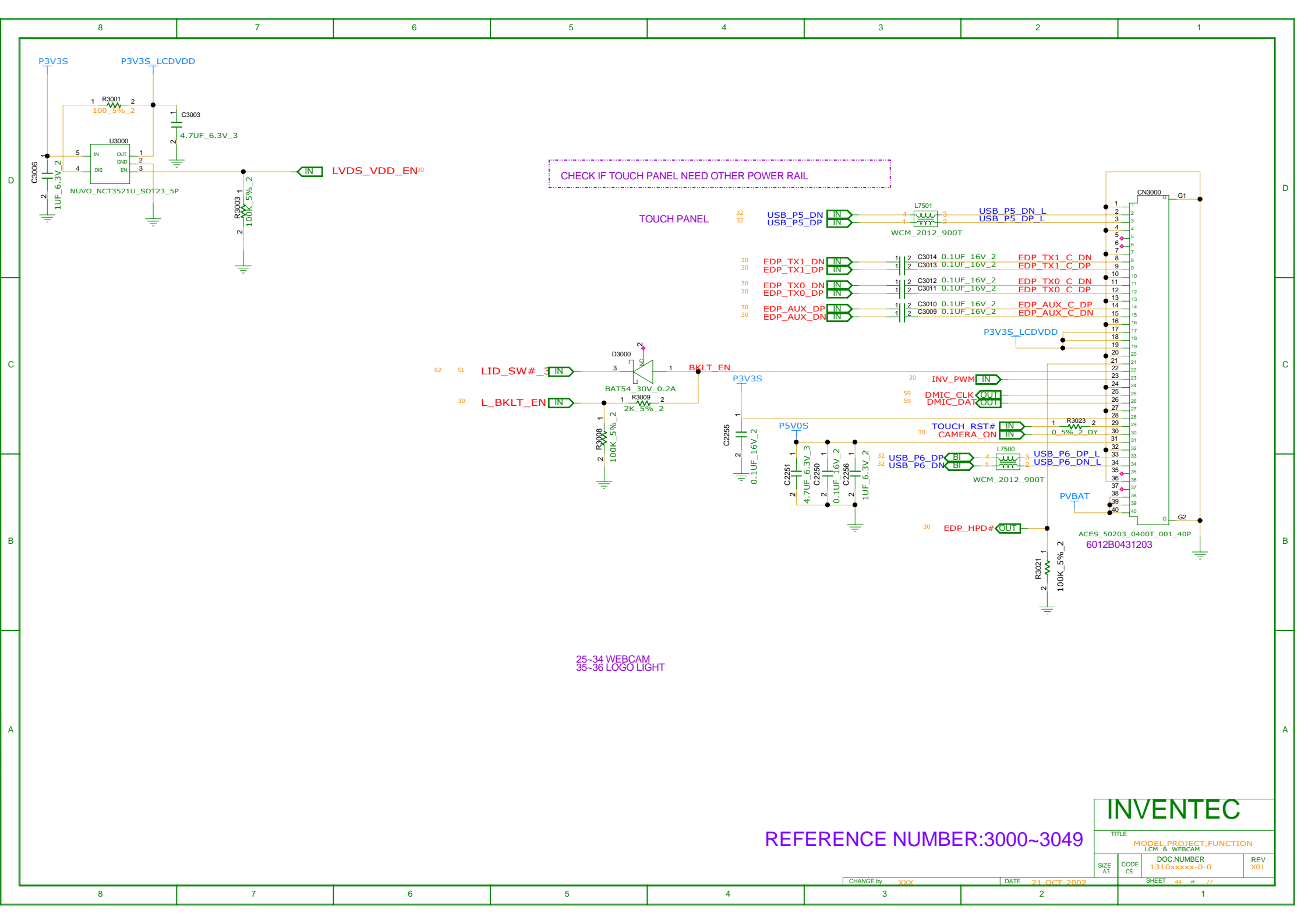
TITLE			
MODEL PROJECT FUNCTION DPC DEMUX2 TO VGA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 41 of 77			





REFERENCE NUMBER:3300~3399

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
CRT & DP			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 43 of 77			



CHECK IF TOUCH PANEL NEED OTHER POWER RAIL

25~34 WEBCAM
35~36 LOGO LIGHT

REFERENCE NUMBER:3000~3049

INVENTEC			
TITLE MODEL PROJECT,FUNCTION LCM & WEBCAM			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX DATE 21-OCT-2002 SHEET 44 of 77			

REFERENCE NUMBER:1700~1749

REFERENCE NUMBER:1950~1999

M TYPE
6026B0240301
NGFF SSD

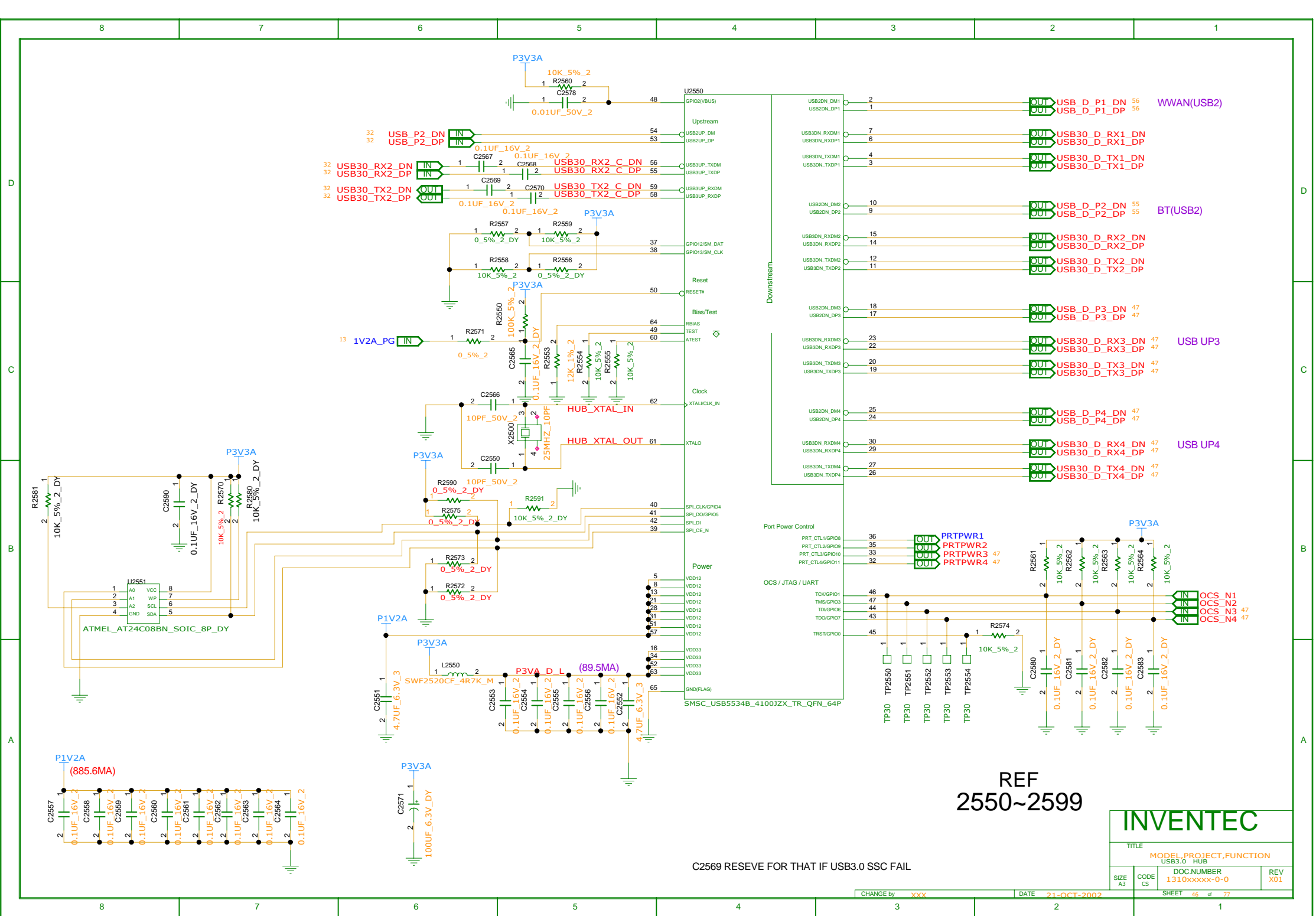
SATA HDD CONNECTOR

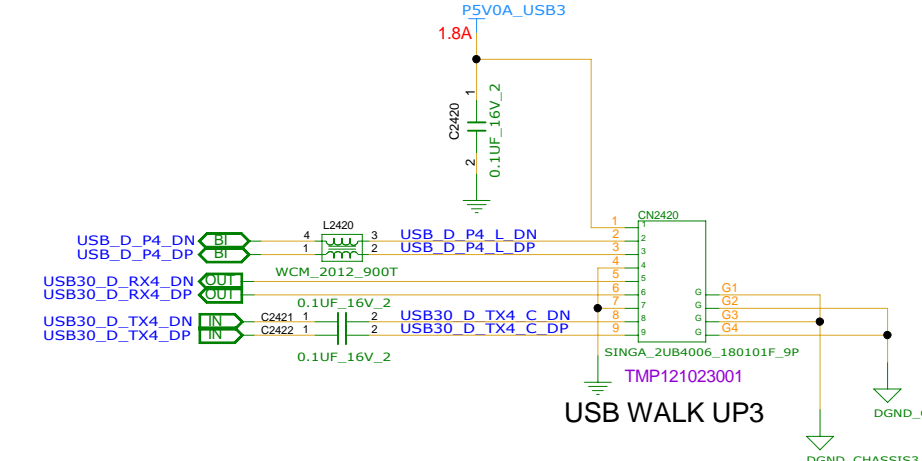
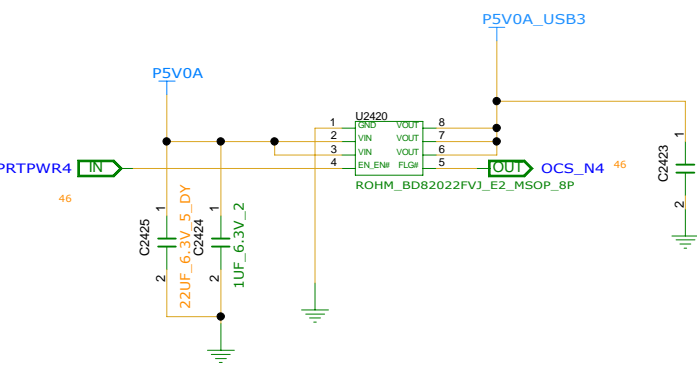
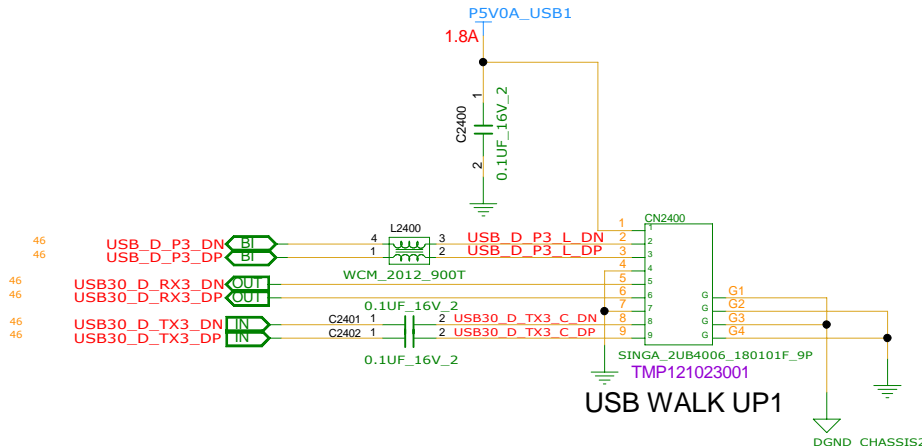
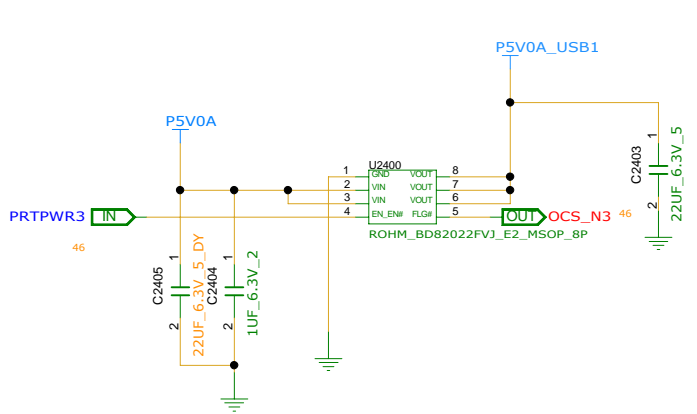
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SATA1_HDD & M-SATA_CONN.

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002 SHEET 45 of 77



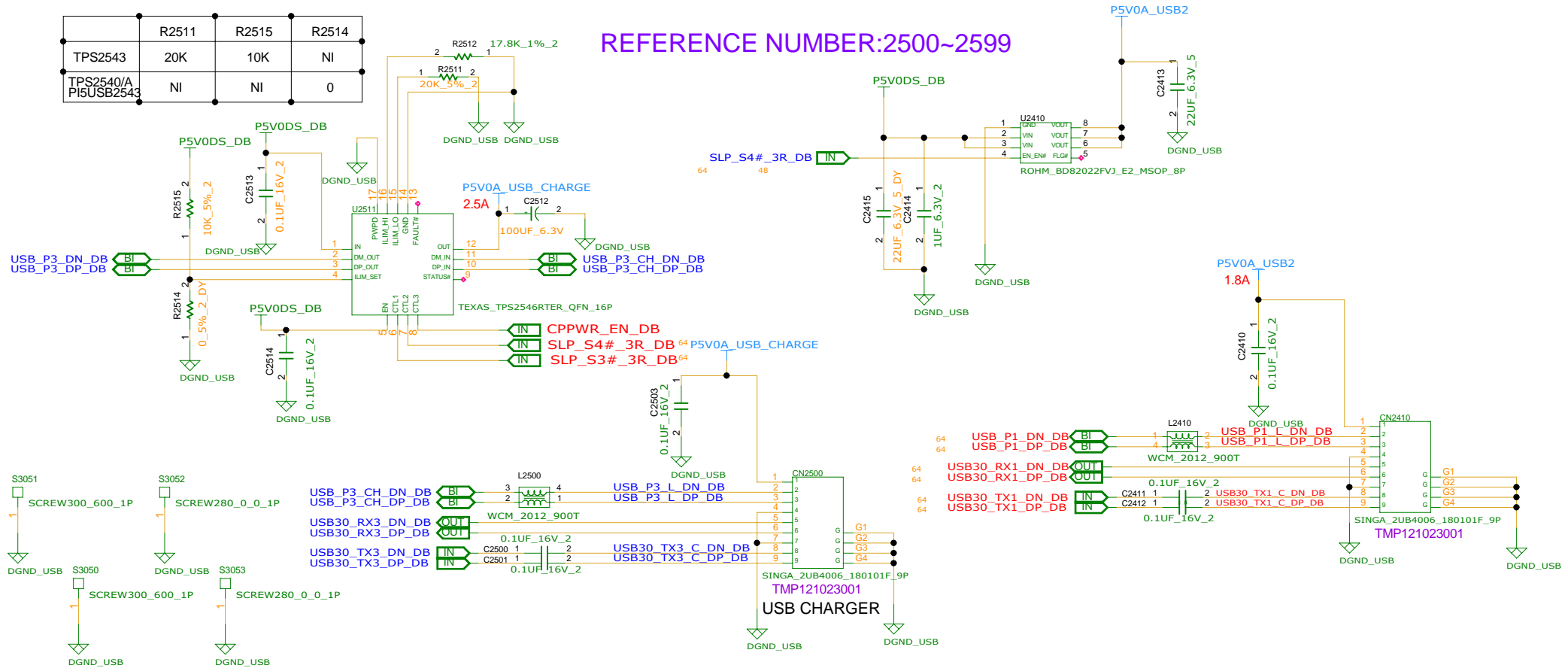


REFERENCE NUMBER:2400~2499

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
USB & USB CHARGER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXXX			
DATE 21-OCT-2002			
SHEET 47 of 77			

	R2511	R2515	R2514
TPS2543	20K	10K	NI
TPS2540/A PI5USB2543	NI	NI	0

REFERENCE NUMBER:2500~2599

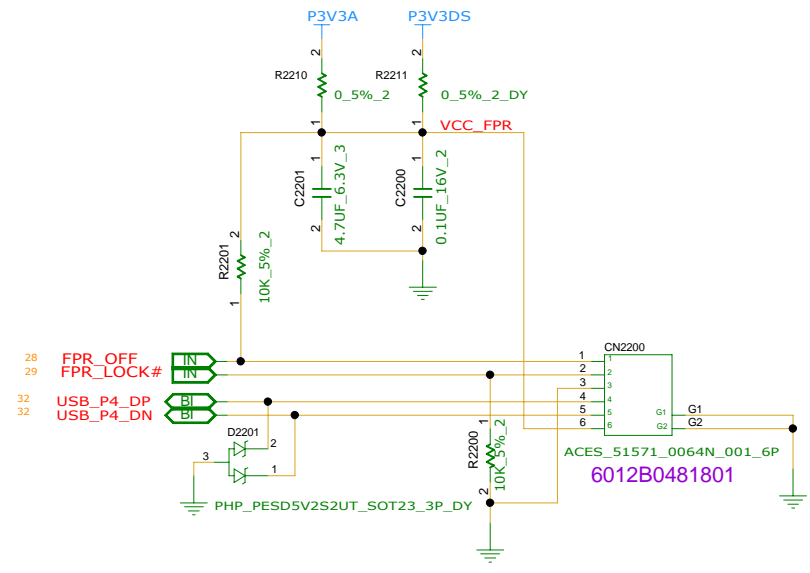


REFERENCE NUMBER:3050~3099

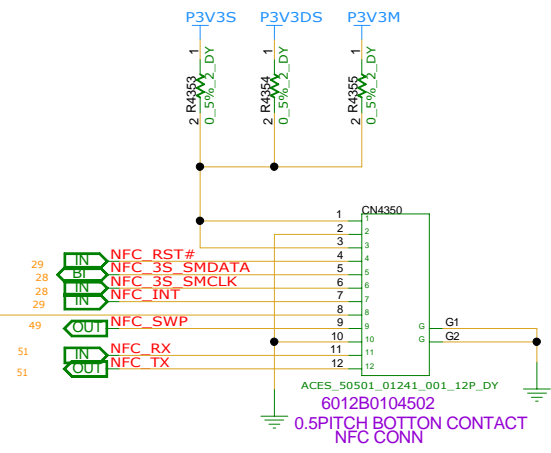
CRT

INVENTEC

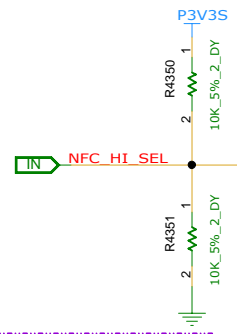
TITLE			
MODEL PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 48 of 77			



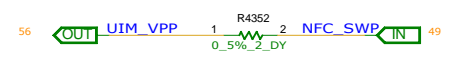
FINGER PRINT CONN



0.5PITCH BOTTOM CONTACT
NFC CONN



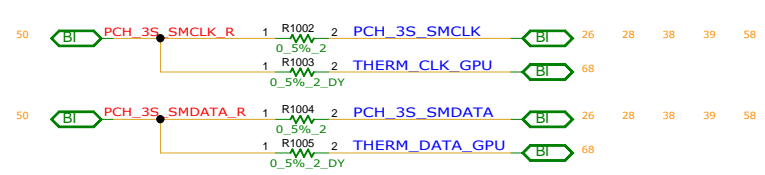
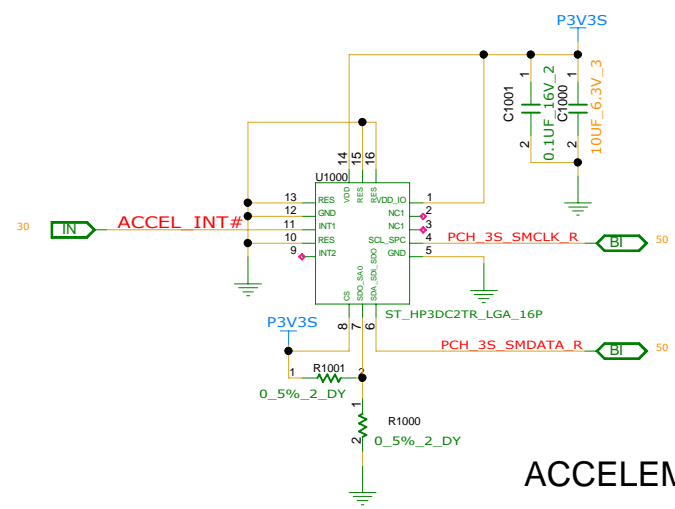
NFC_HI_SEL R4350 R4351
HIGH (UART) INSTALL
LOW (I2C) INSTALL



REFERENCE:2200~2249

REFERENCE:4350~4399

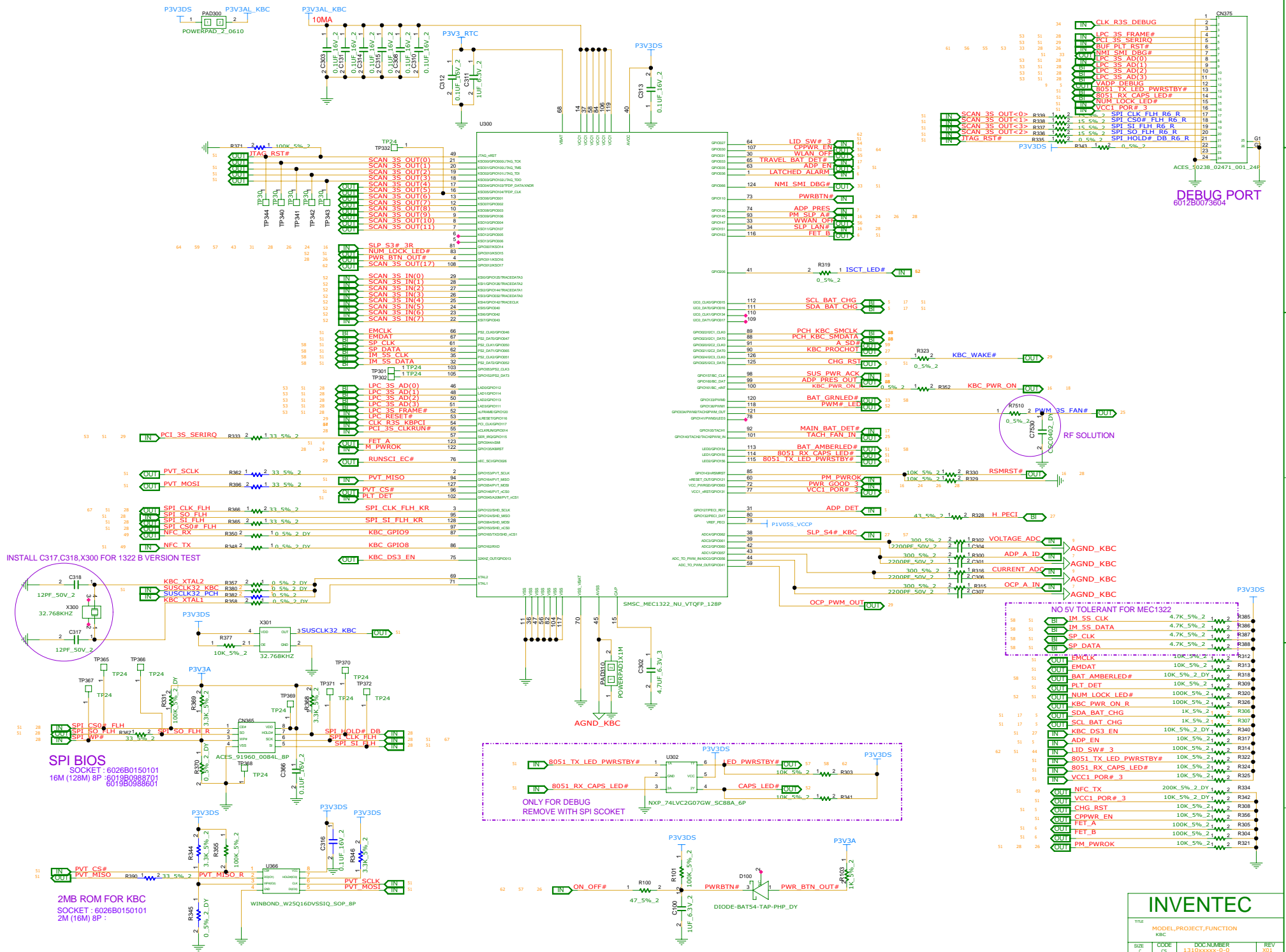
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
FINGER PRINTER & NFC			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 49 of 77			



REFERENCE NUMER : 1000~1099

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION ACCELEMATOR			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 50 of 77

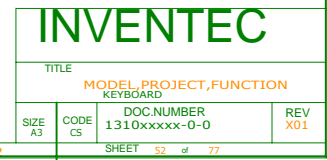
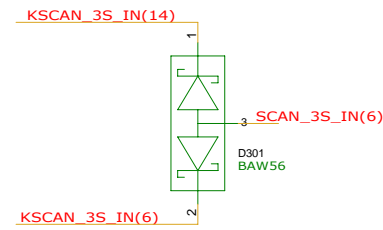
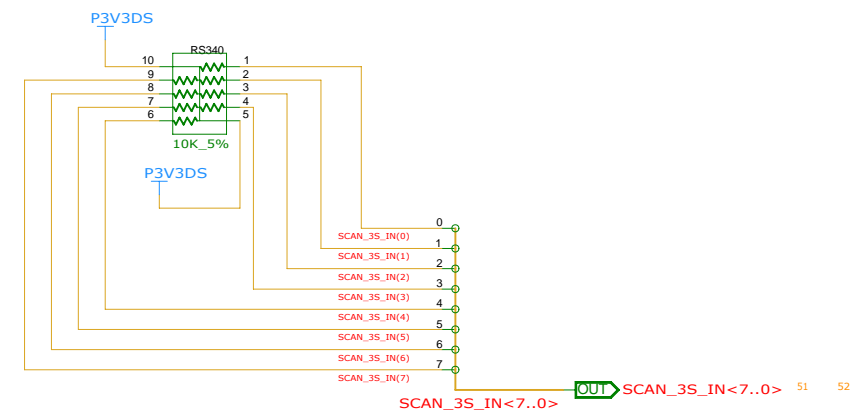
REFERENCE NUMBER : 300~399

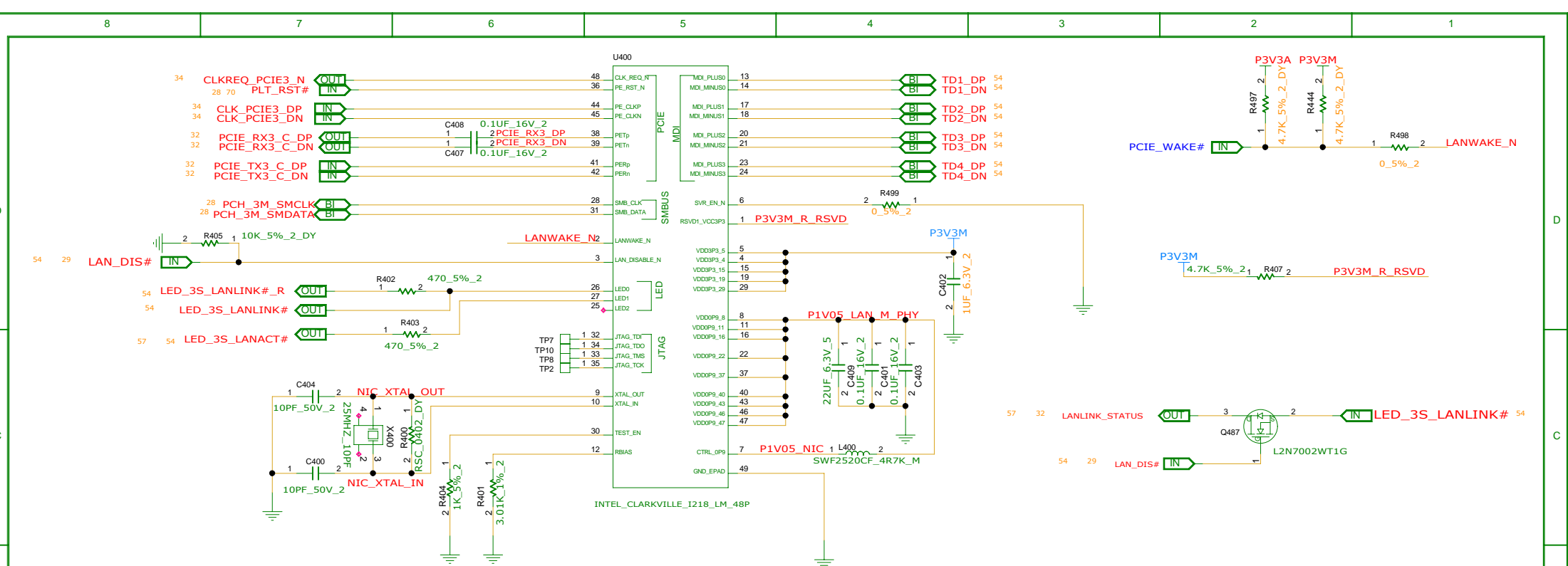


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
KBC			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

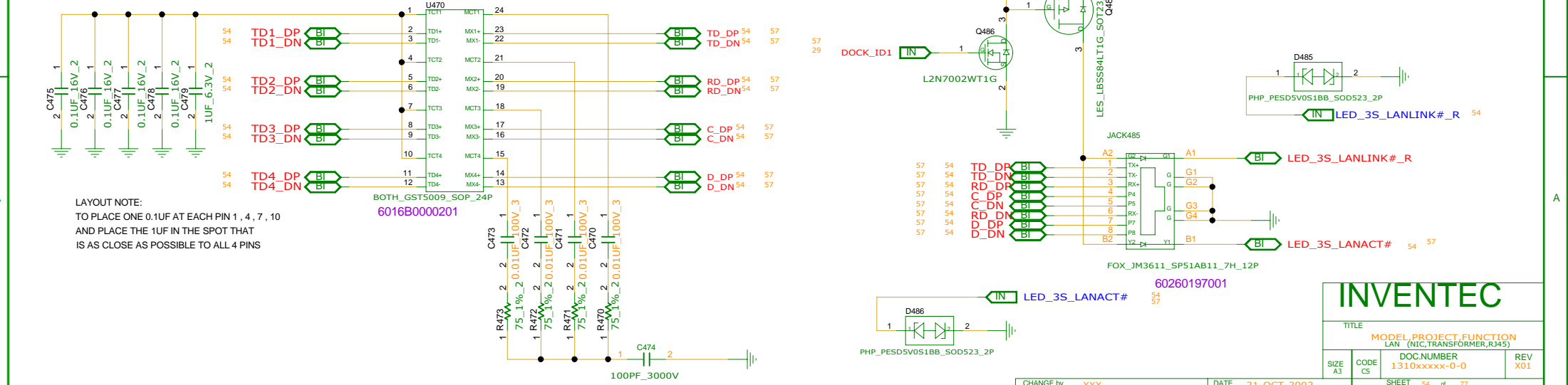
A





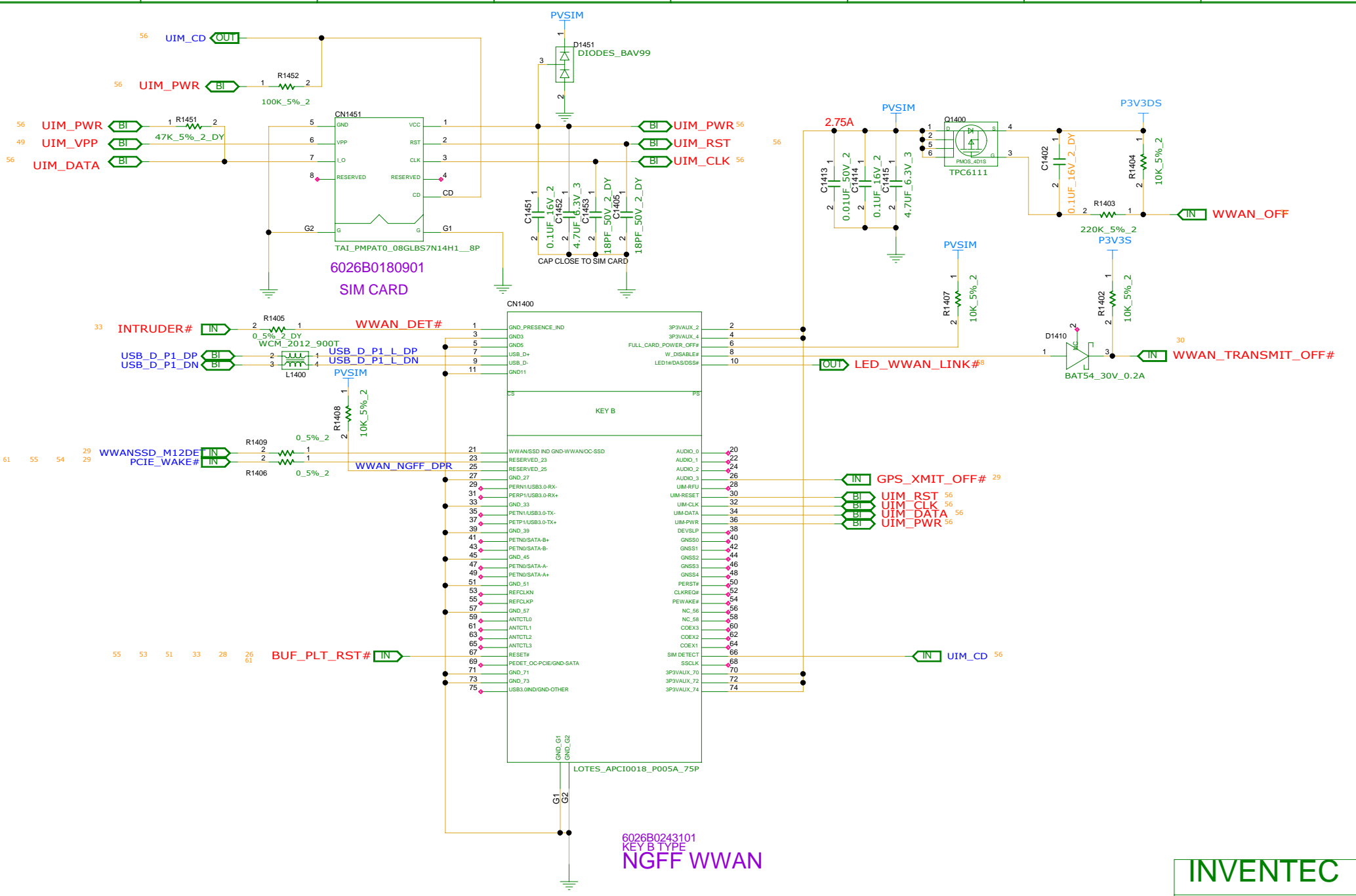
REFERENCE NUMER : 400~469

REFERENCE NUMER : 470~499



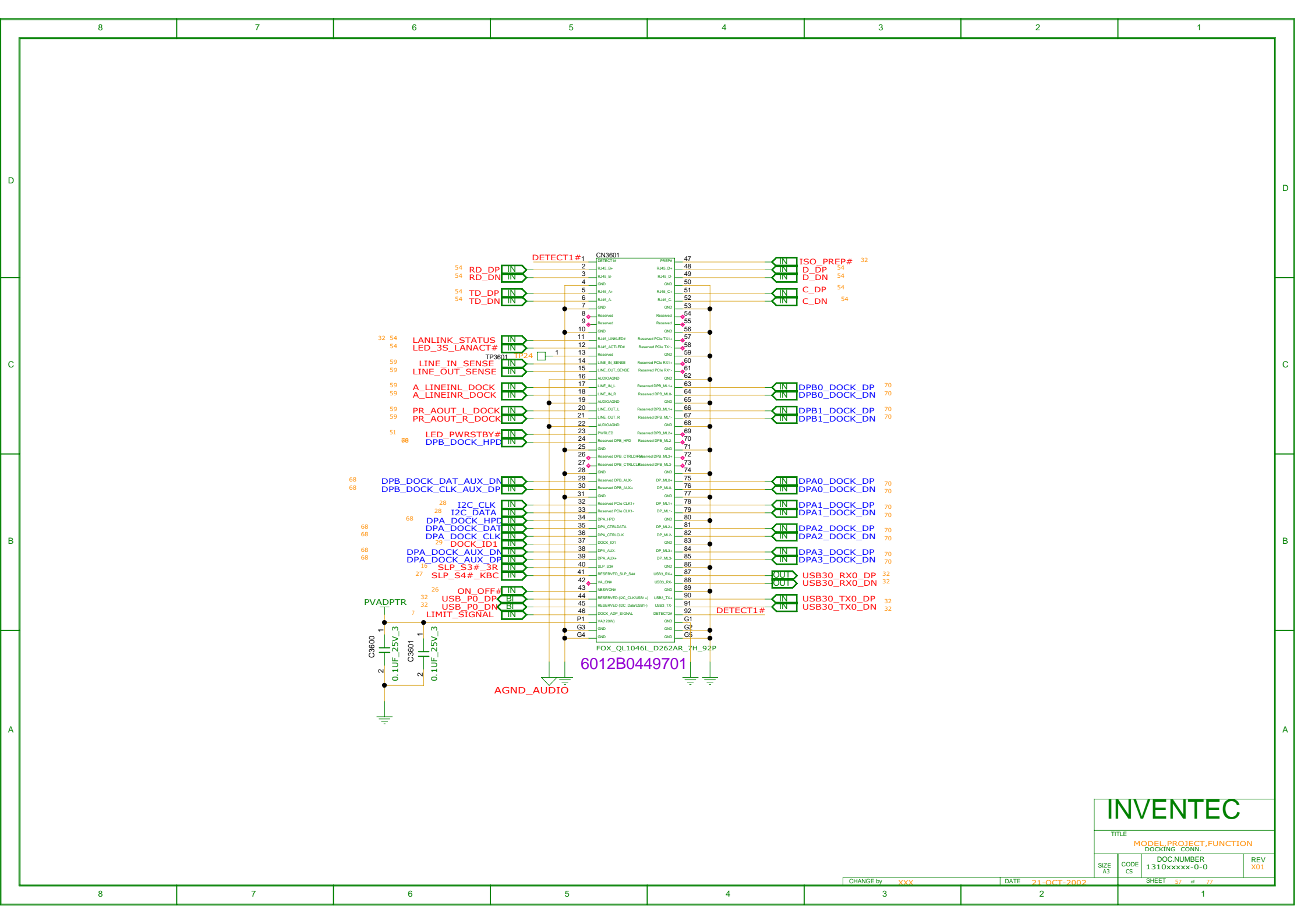
LAYOUT NOTE:
TO PLACE ONE 0.1UF AT EACH PIN 1, 4, 7, 10
AND PLACE THE 1UF IN THE SPOT THAT
IS AS CLOSE AS POSSIBLE TO ALL 4 PINS

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
LAN (NIC, TRANSFORMER, RJ45)			
DOC NUMBER			
1310xxxxx-0-0			
REV			
X01			
SIZE	CODE	SHEET	
A3	CS	54 of 77	



REFERENCE NUMBER:1400~1499

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
WWAN NGFF			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 56 of 77			

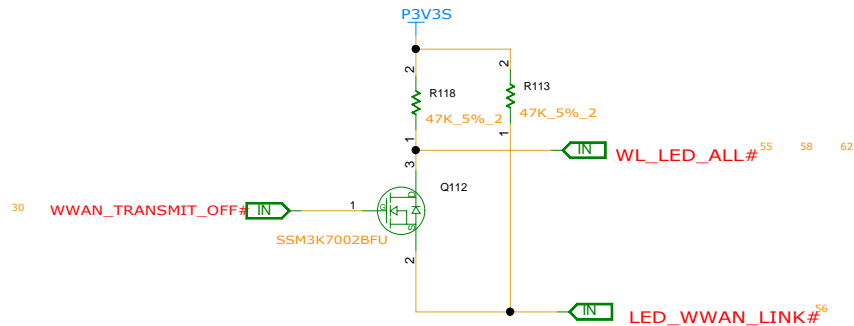


INVENTEC

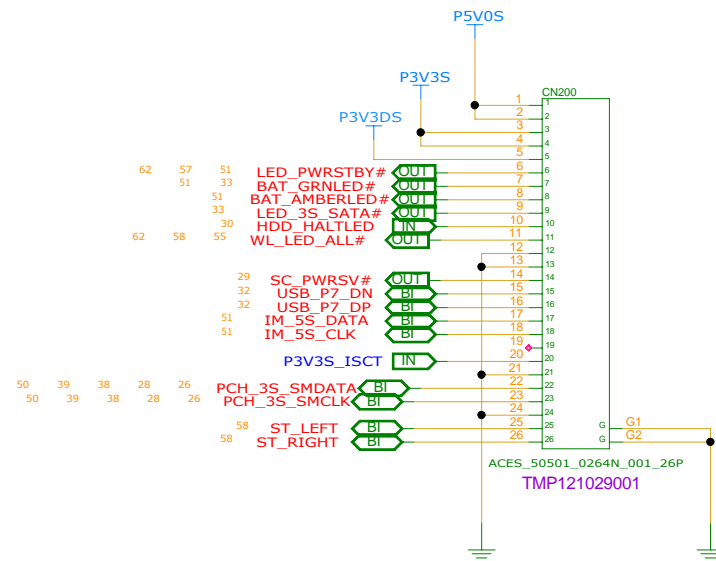
TITLE
MODEL PROJECT,FUNCTION
DOCKING CONN.

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

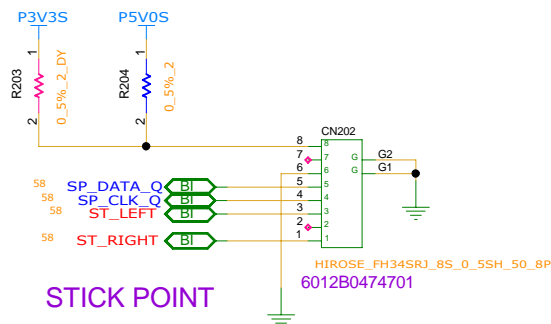
CHANGE by XXX DATE 21-OCT-2002 SHEET 57 of 77



WLAN_WWAN_BLUETOOTH_LED

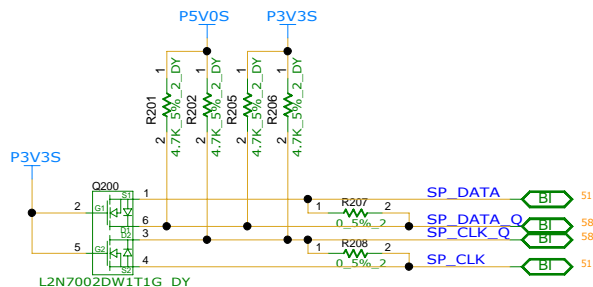


SMART CARD AND TOUCHPAD D/B W TO B CONN



STICK POINT

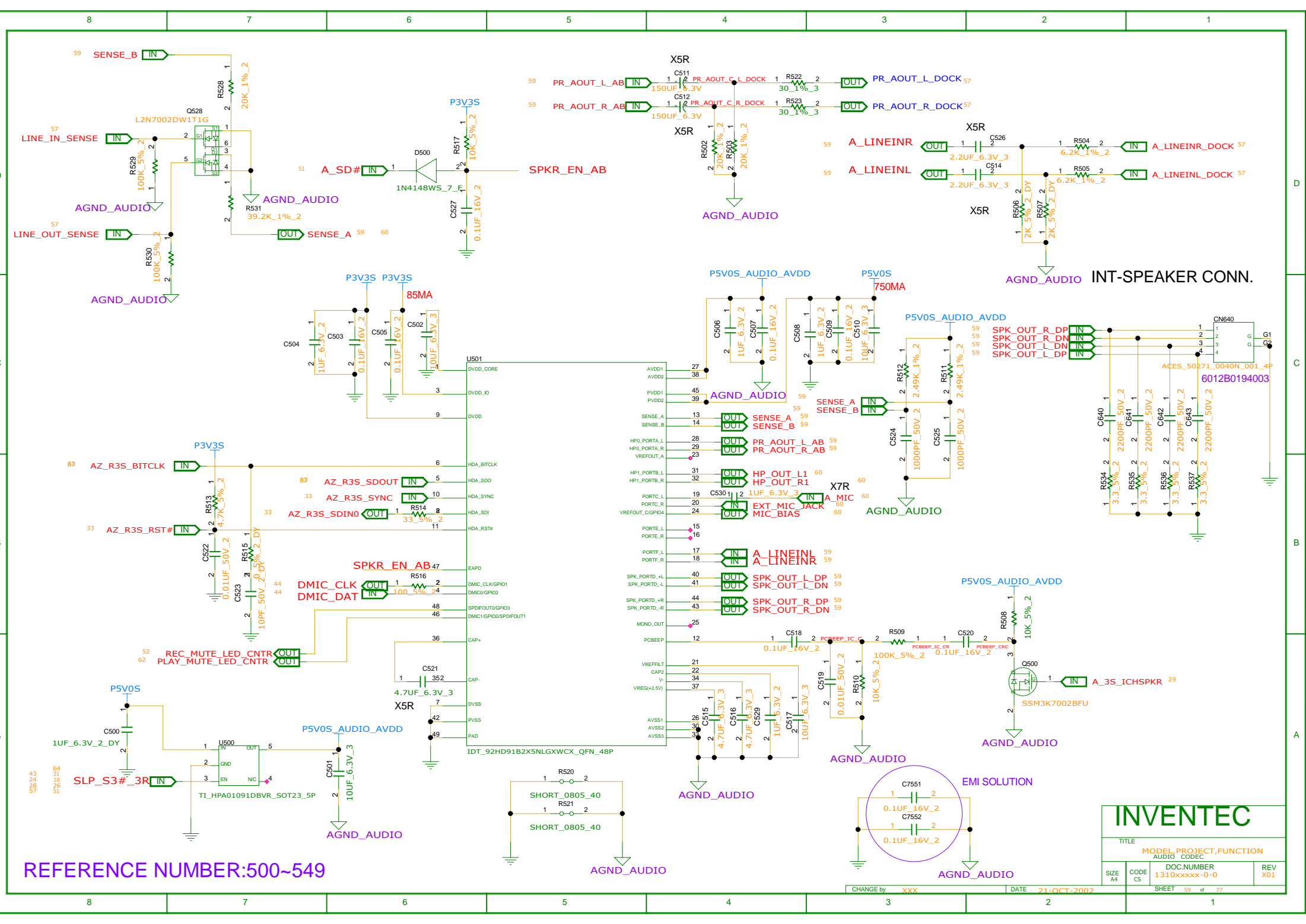
	5V	3.3V
R201	INSTALL	UNINSTALL
R202	INSTALL	UNINSTALL
R203	UNINSTALL	INSTALL
R204	INSTALL	UNINSTALL



STICK POINT OPTION

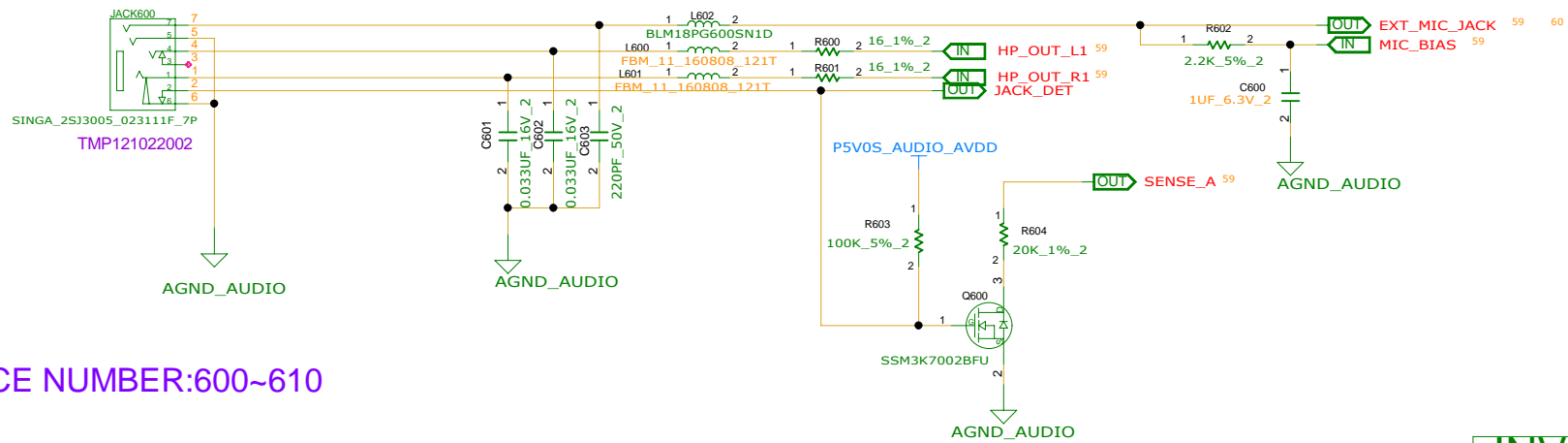
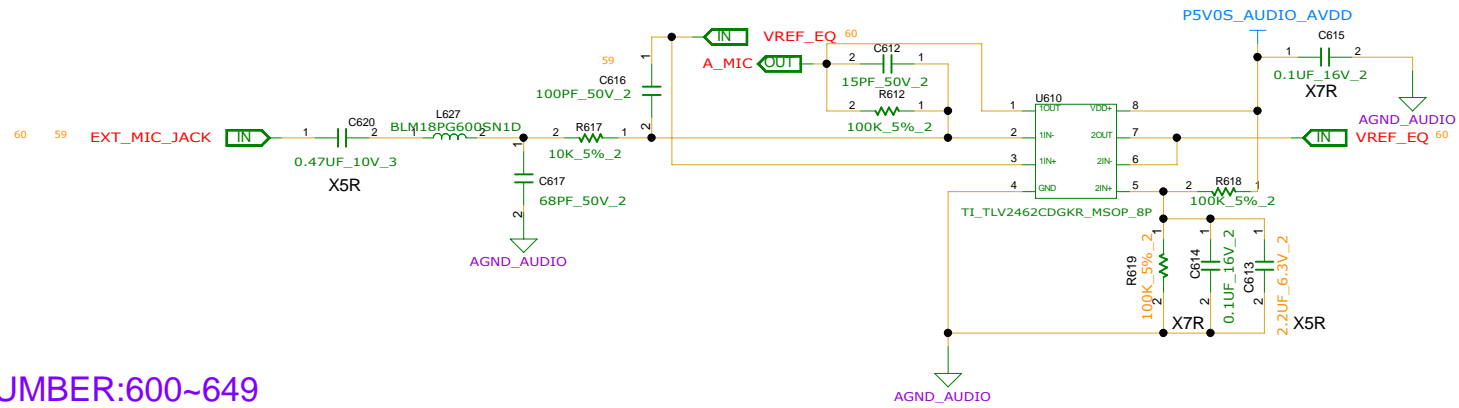
REFERENCE NUMBER:100~199

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
STICK POINT & B2B CNTR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 58 of 77			



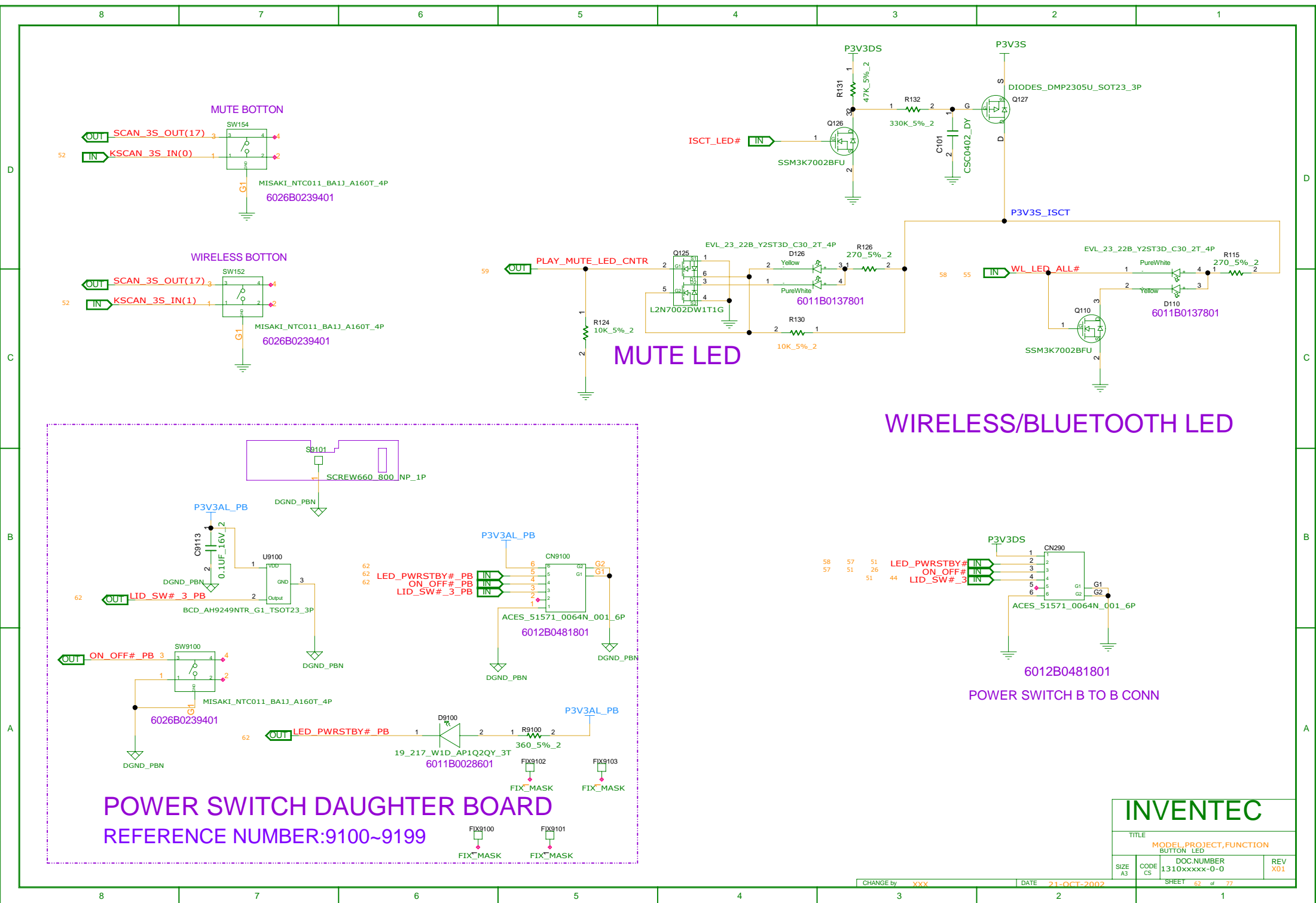
REFERENCE NUMBER:500~549

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
AUDIO CODEC			
DOC NUMBER			
1310xxxxx-0-0			
REV			
X01			
SIZE	CODE	DATE	
A4	CS	21-OCT-2002	
CHANGE by		XXX	
SHEET		59	of 77



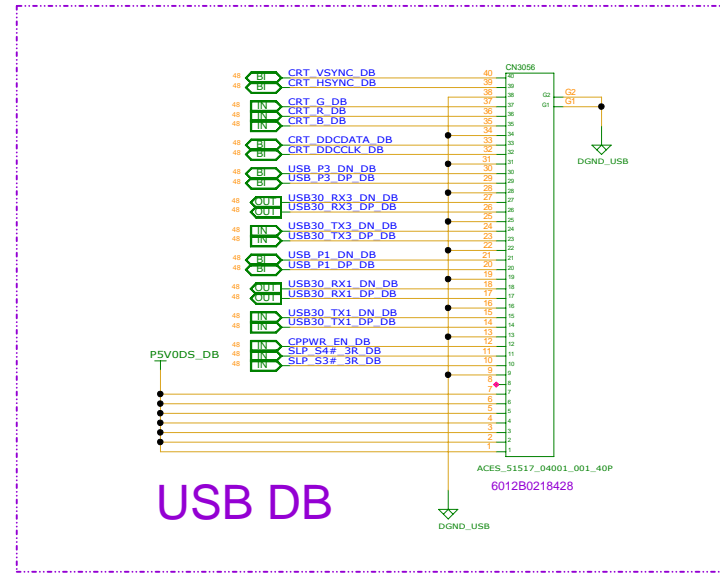
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION EXT. MIC AMP. & AUDIO JACK			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 60 of 77			

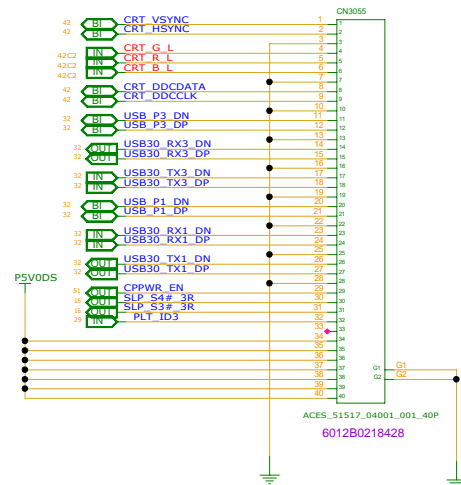


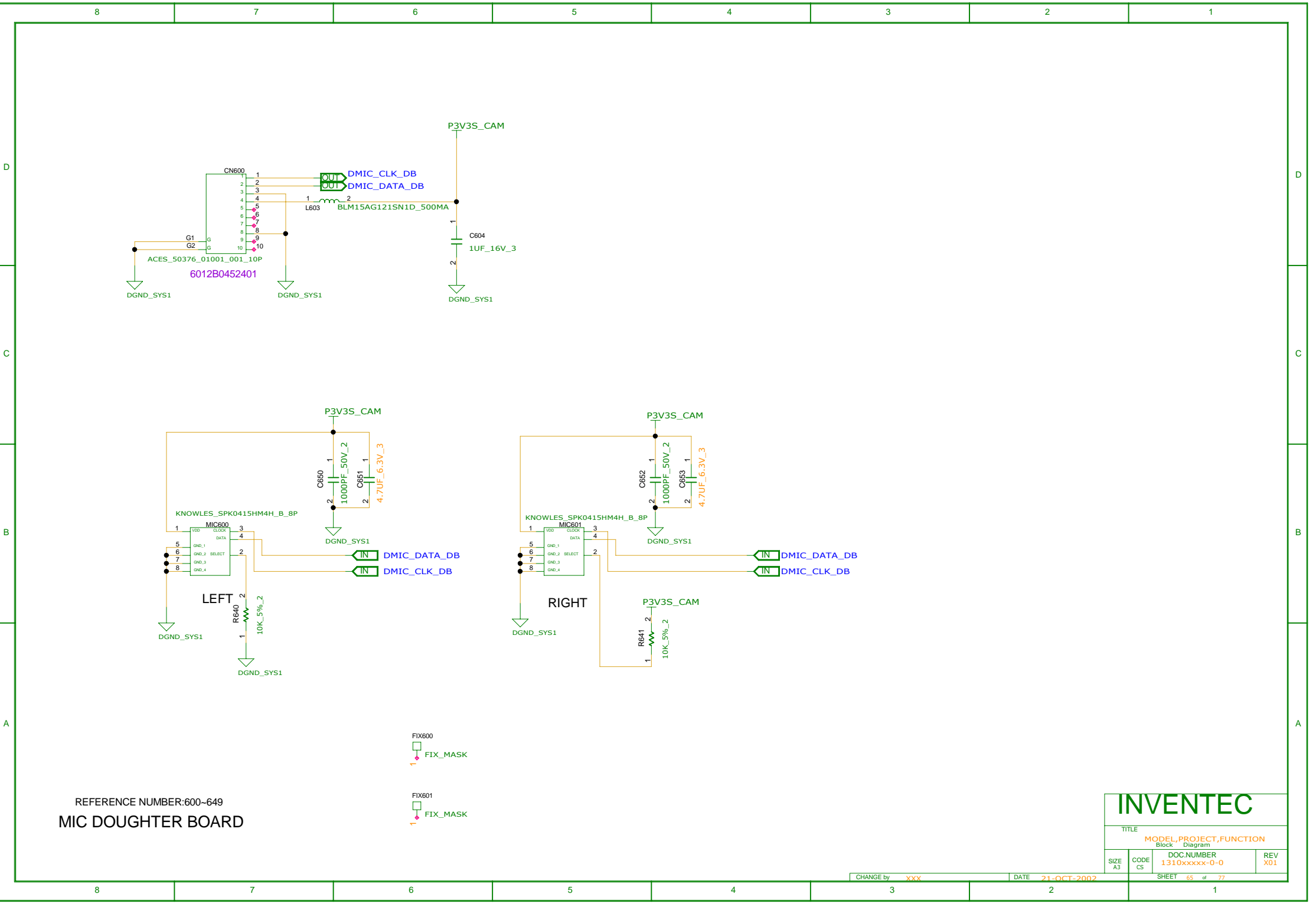
POWER SWITCH DAUGHTER BOARD
REFERENCE NUMBER:9100~9199

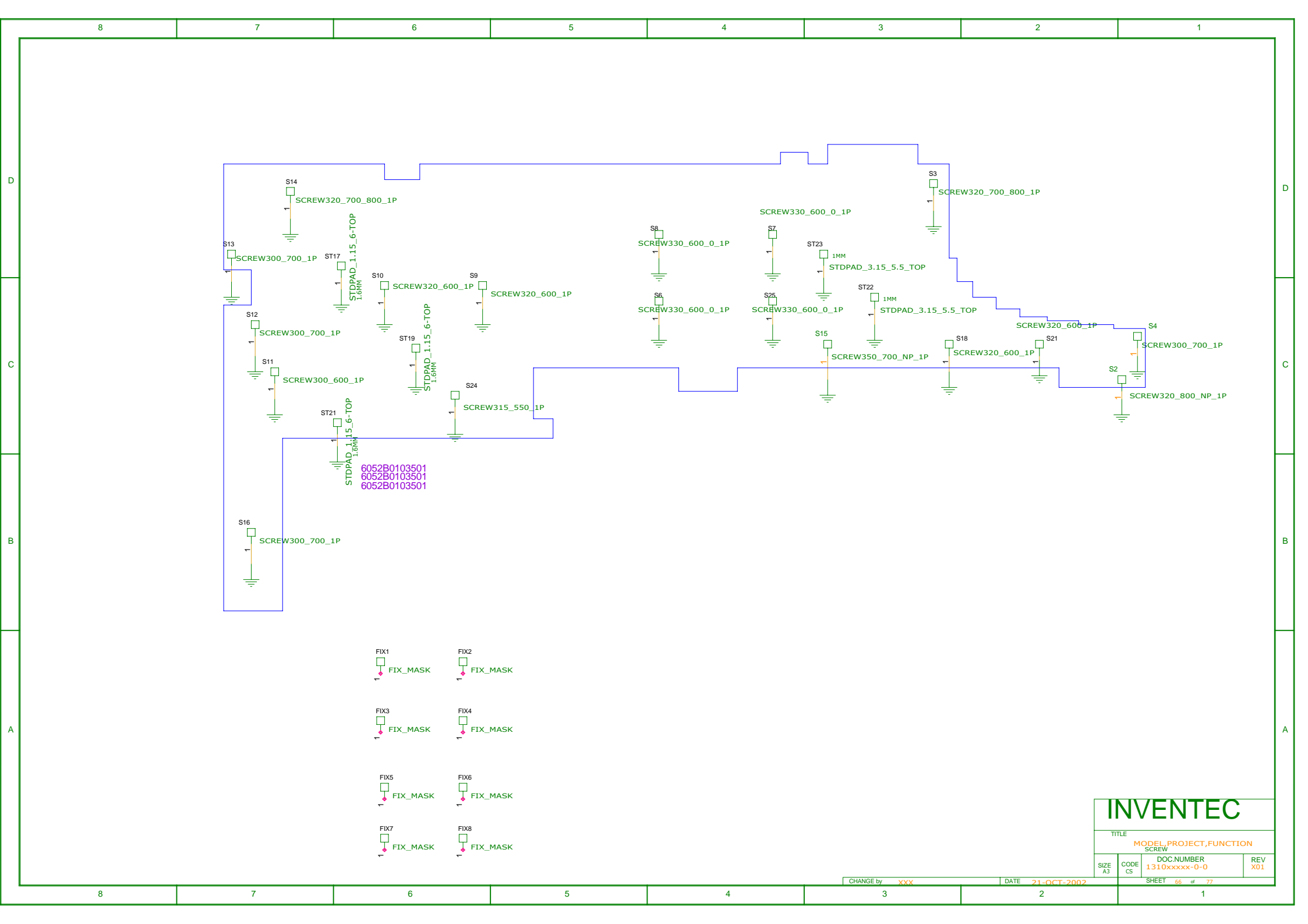
INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
SIZE A3	CODE C3	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 62 of 77			

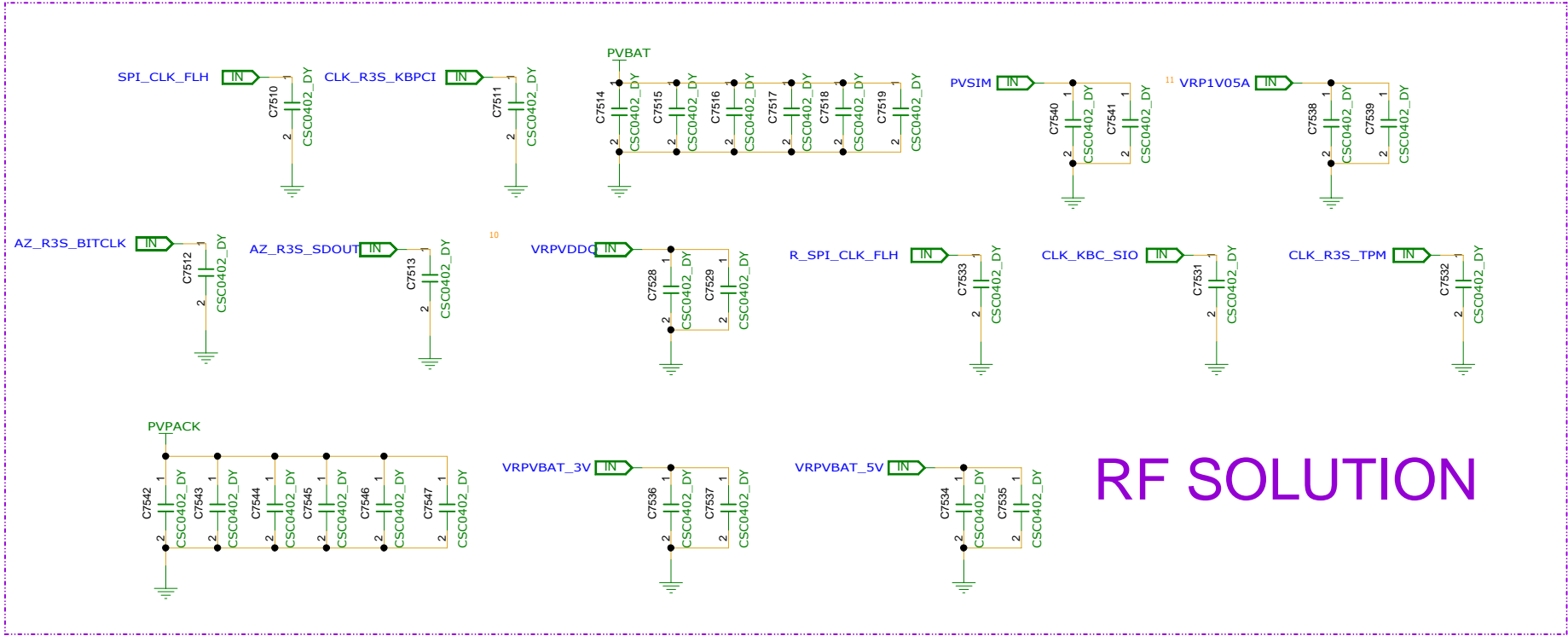


USB DB

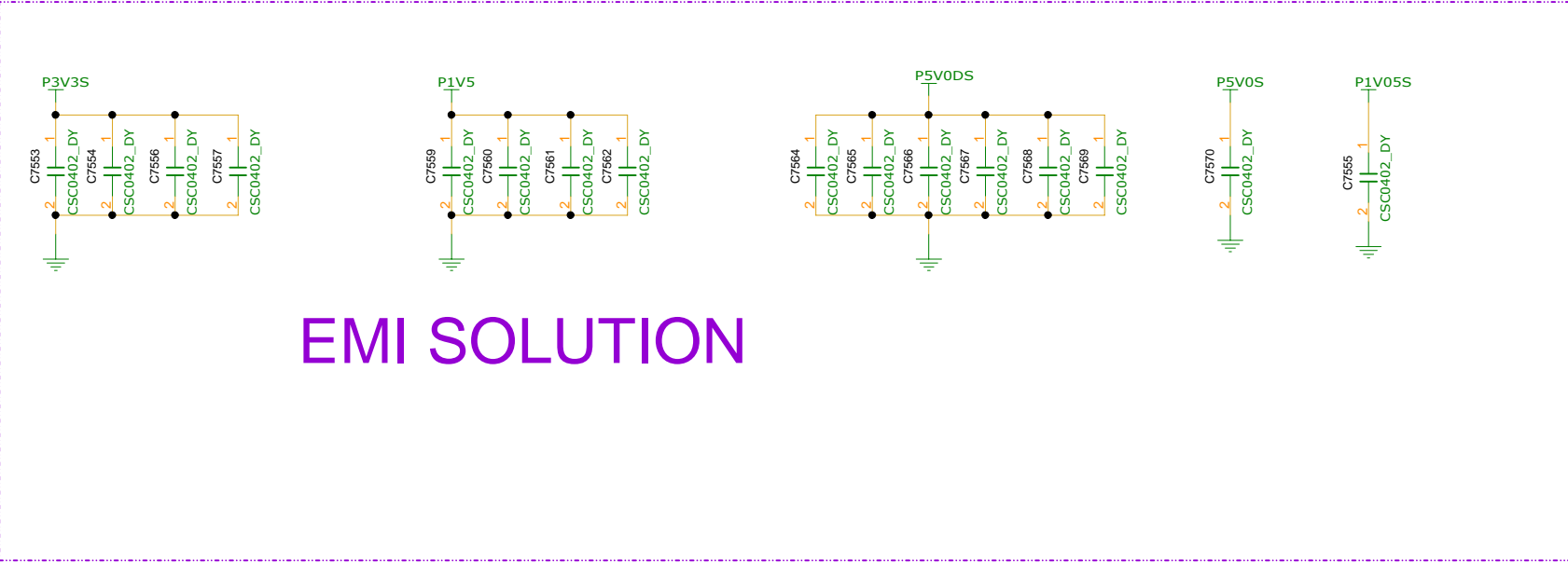








RF SOLUTION



EMI SOLUTION

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
EMI & RF SOLUTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 67 of 77			

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

Note: 0402 1% resistors are required.

Capacitor Value (nF) Bits [5:4]

680	00
82	01
10	10
NC	11

MLPS Configuration:

Pin	Signal	Value
TP30	TP5000	1 GPU_TRSTB
TP30	TP5001	1 GPU_TDI
TP30	TP5002	1 GPU_TCK
TP30	TP5003	1 GPU_TMS
TP30	TP5004	1 GPU_TDO

MLPS Pin Connections:

- P3V3S_DGPU:** P3V3S_DGPU to P3V3S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P1V8S_DGPU:** P1V8S_DGPU to P1V8S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P3V3S:** P3V3S to P3V3S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P1V8S:** P1V8S to P1V8S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- PS:** PS to PS (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- THERM:** THERM to THERM (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

Note: 0402 1% resistors are required.

Capacitor Value (nF) Bits [5:4]

680	00
82	01
10	10
NC	11

MLPS Configuration:

Pin	Signal	Value
TP30	TP5000	1 GPU_TRSTB
TP30	TP5001	1 GPU_TDI
TP30	TP5002	1 GPU_TCK
TP30	TP5003	1 GPU_TMS
TP30	TP5004	1 GPU_TDO

MLPS Pin Connections:

- P3V3S_DGPU:** P3V3S_DGPU to P3V3S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P1V8S_DGPU:** P1V8S_DGPU to P1V8S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P3V3S:** P3V3S to P3V3S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- P1V8S:** P1V8S to P1V8S (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- PS:** PS to PS (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).
- THERM:** THERM to THERM (R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034).

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

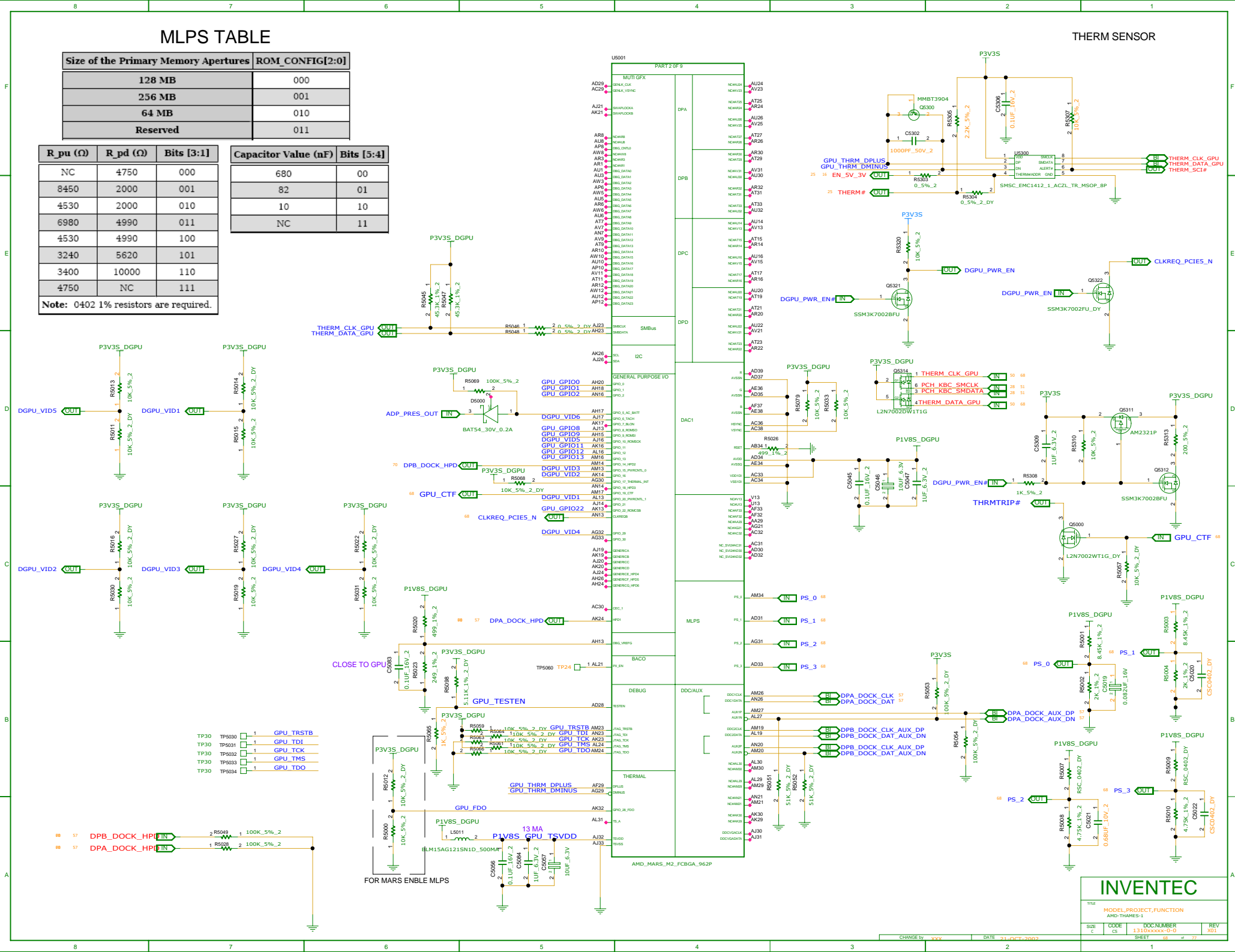
Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

INVENTEC

MODEL	PROJECT	FUNCTION
AMD-THAMES-1		
SIZE	CODE	DOC NUMBER
C	15	1310-XXXX-10-10
SHEET	68	of 77
REV	001	



MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

The schematic diagram illustrates the internal components and signal traces of the AMD-THAMES-1 MLPS board. Key components include:

- MLPS TABLE:** A table defining the relationship between memory aperture sizes and ROM configuration bits.
- Capacitor Value Table:** A table mapping capacitor values to specific bit patterns.
- THERM SENSOR:** A section detailing the thermal sensor circuitry, including the THERM_CLK_GPU and THERM_DATA_GPU signals.
- Connectors:** Various connectors are shown, including the GPU_FDO, GPU_TRSTB, GPU_TCK, GPU_TMS, and GPU_TDO.
- Signal Traces:** The diagram shows the routing of signals such as GPU_THRM_DPLUS, GPU_THRM_DMINUS, GPU_FDO, GPU_TRSTB, GPU_TCK, GPU_TMS, and GPU_TDO.
- Power and Ground:** Power planes (P3V3S, P1V8S) and ground connections are indicated throughout the board.

INVENTEC

TITLE	MODEL_PROJECT_FUNCTION
AMD-THAMES-1	
SIZE	CODE
C	15
SHEET	68
REV	001

[illegible]

LPT-LP GPIO 34	MARS MLPS Bit: PS_3 [3:1]			R_pu (Ω)	R_pd (Ω)	Vendor & PN	Die Ver.	
0	0	0	0	NC	4750	Samsung - K4G20325FD-FC04	D	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	0	0	1	8450	2000	Hynix - H5GQ2H24AFR-T2C	A (Gemma)	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
1	1	1	0	3400	10000	*Samsung - K4G41325FC-HC04	C	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	1	1	1	4759	NC	*Hynix - H5GC4H24MFR-T0C	Huma	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
VBIOS selection : 0 : VBIOS 1, 64Mx32 for 1GB sku 1 : VBIOS 2, 128Mx32 for 2GB sku	Vram configuration 00: 64Mx32 (2Gb) 11: 128Mx32 (4Gb)		Vendor ID 0: Samsung 1: Hynix	Resistor Divider Lookup Table		Vram information * 2GB sku, TBD		

MLPS Implementation

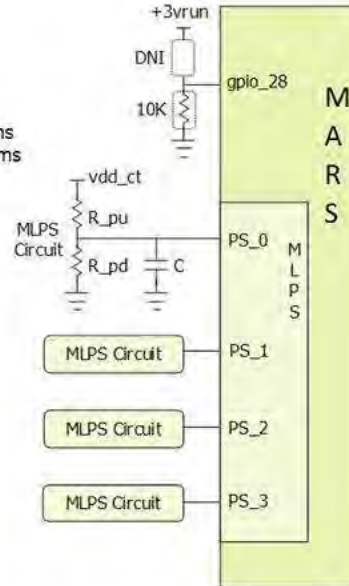
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



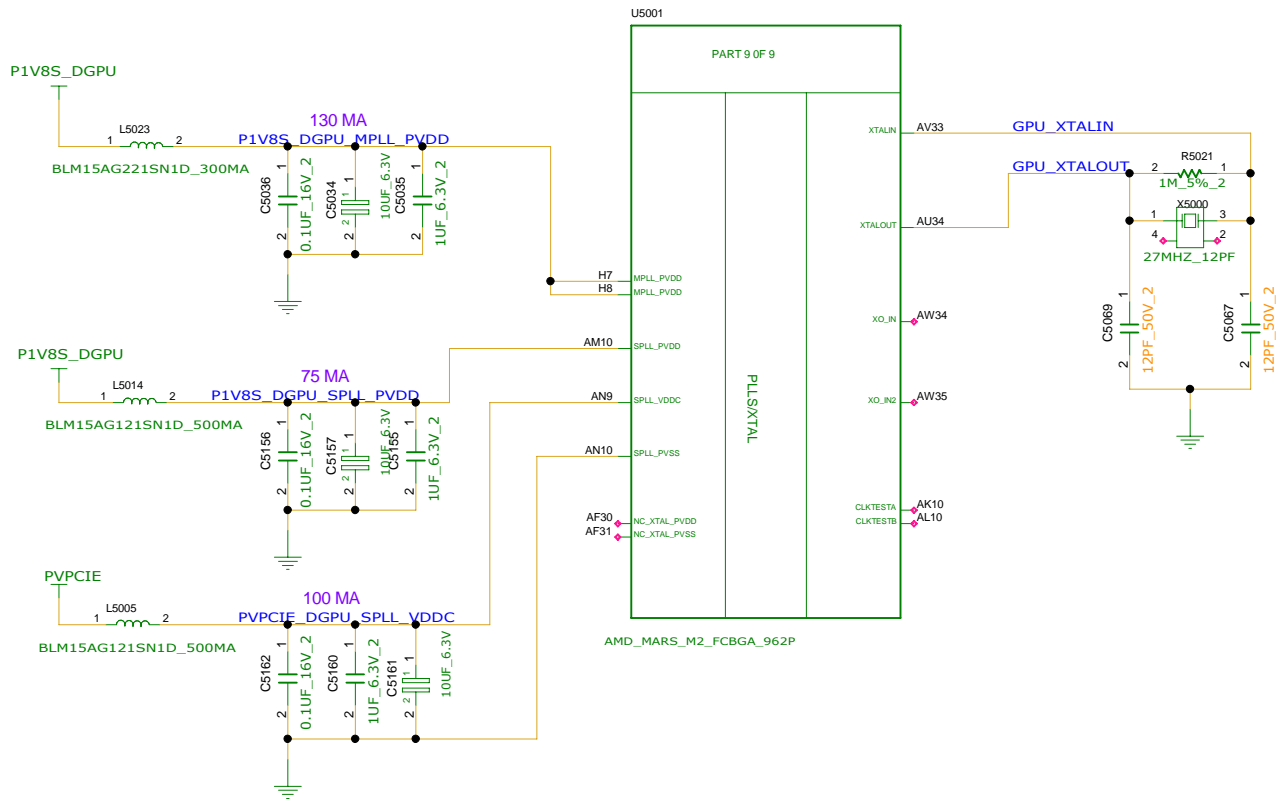
MLPS Bit	Strap Name	Description
PS_0[1]	ROM_CONFIG[0]	See Primary Memory Aperture Sizes.
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 1 = Tx deemphasis enabled.
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_3[1]	BOARD_CONFIG[0]	See Board configuration related strapping, such as for memory ID.
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	

Note : AUD[1] (on HYSNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2] PS_3[4] PS_0[5]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

INVENTEC

MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXX-0-0	201
SHEET		68	of 77

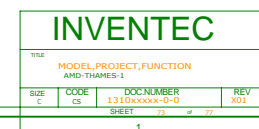


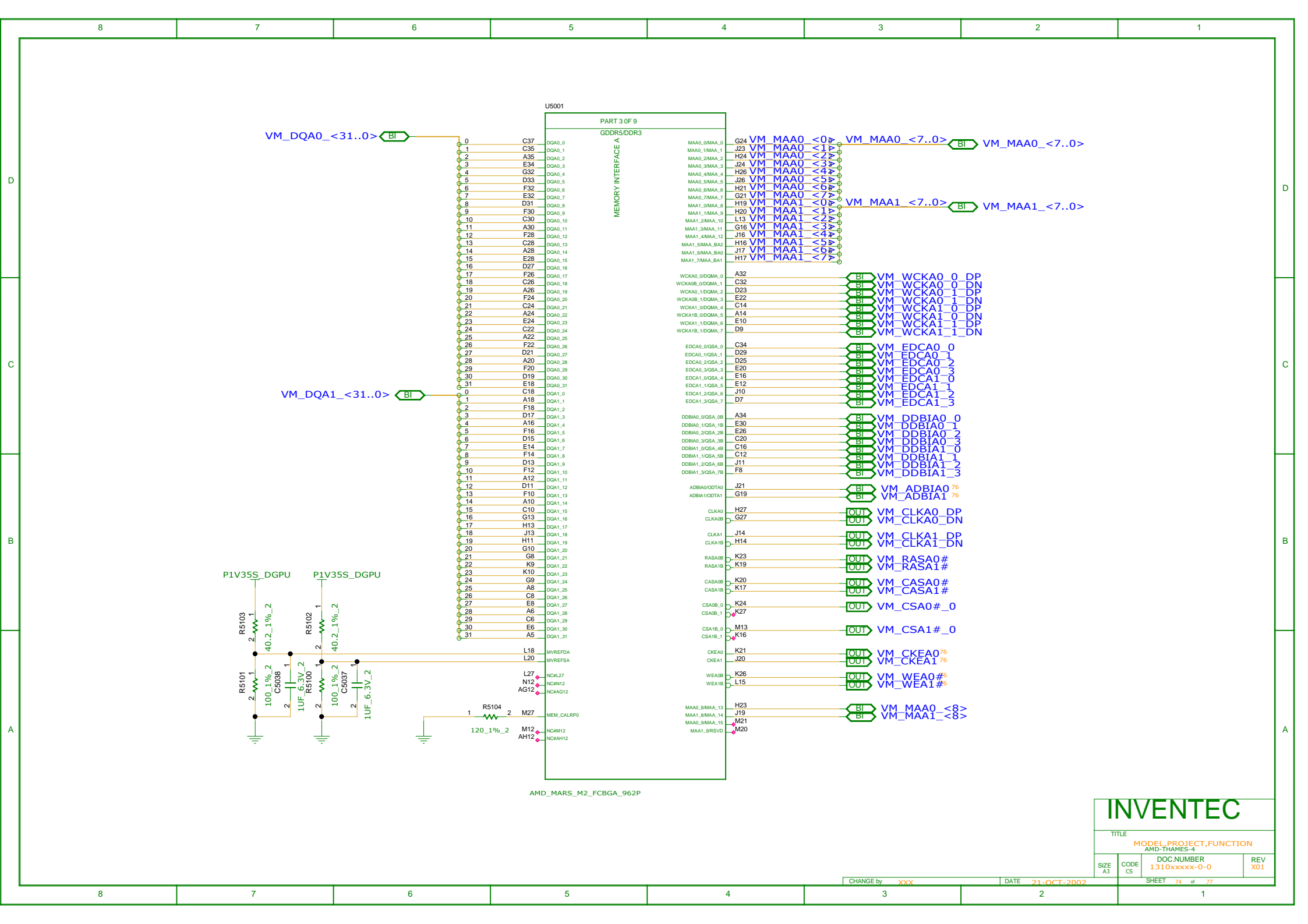
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 21 of 77





INVENTEC

TITLE
MODEL PROJECT FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 74 of 77

VM_DQB0_<31..0>

VM_DQB1_<31..0>

P1V35S_DGPU

P1V35S_DGPU

AMD_MARS_M2_FCBGA_962P

U5001

PART 4 OF 9

GDDBS/DDR3

MEMORY INTERFACE B

MAB0_0MAB0_0
MAB0_1MAB0_1
MAB0_2MAB0_2
MAB0_3MAB0_3
MAB0_4MAB0_4
MAB0_5MAB0_5
MAB0_6MAB0_6
MAB0_7MAB0_7
MAB0_8MAB0_8
MAB1_1MAB1_1
MAB1_2MAB1_2
MAB1_3MAB1_3
MAB1_4MAB1_4
MAB1_5BA2
MAB1_6BA0
MAB1_7BA1

WCKB0_0DQMB_0
WCKB0B_0DQMB_1
WCKB0_1DQMB_2
WCKB0B_1DQMB_3
WCKB1_0DQMB_4
WCKB1B_0DQMB_5
WCKB1_1DQMB_6
WCKB1B_1DQMB_7

EDCB0_0QSB_0
EDCB0_1QSB_1
EDCB0_2QSB_2
EDCB0_3QSB_3
EDCB1_0QSB_4
EDCB1_1QSB_5
EDCB1_2QSB_6
EDCB1_3QSB_7

DDBB0_0QSB_0B
DDBB0_1QSB_1B
DDBB0_2QSB_2B
DDBB0_3QSB_3B
DDBB1_0QSB_4B
DDBB1_1QSB_5B
DDBB1_2QSB_6B
DDBB1_3QSB_7B

ADBIB0_0DTB0
ADBIB1_0DTB1

CLKB0
CLKB0B
CLKB1
CLKB1B

RASB0B
RASB1B

CASB0B
CASB1B

CSB0B_0
CSB0B_1

CSB1B_0
CSB1B_1

CKEB0
CKEB1

WEB0B
WEB1B

MAB0_8MAB0_13
MAB1_8MAB1_14
MAB0_9MAB0_15
MAB1_9RSVD

DRAM_RST

VM MAB0 <0> VM MAB0 <7..0>

VM MAB0 <1> VM MAB0 <2>

VM MAB0 <3> VM MAB0 <4>

VM MAB0 <5> VM MAB0 <6>

VM MAB0 <7> VM MAB0 <8>

VM MAB1 <0> VM MAB1 <7..0>

VM MAB1 <1> VM MAB1 <2>

VM MAB1 <3> VM MAB1 <4>

VM MAB1 <5> VM MAB1 <6>

VM MAB1 <7> VM MAB1 <8>

VM WCKB0_0 DP

VM WCKB0_0 DN

VM WCKB0_1 DP

VM WCKB0_1 DN

VM WCKB1_0 DP

VM WCKB1_0 DN

VM WCKB1_1 DP

VM WCKB1_1 DN

VM EDCB0_0

VM EDCB0_1

VM EDCB0_2

VM EDCB0_3

VM EDCB1_0

VM EDCB1_1

VM EDCB1_2

VM EDCB1_3

VM DDBIB0_0

VM DDBIB0_1

VM DDBIB0_2

VM DDBIB0_3

VM DDBIB1_0

VM DDBIB1_1

VM DDBIB1_2

VM DDBIB1_3

VM ADBIB0_77

VM ADBIB1_77

VM CLKB0_DP

VM CLKB0_DN

VM CLKB1_DP

VM CLKB1_DN

VM RASB0#

VM RASB1#

VM CASB0#

VM CASB1#

VM CSB0#_0

VM CSB1#_0

VM CKEB0_77

VM CKEB1_77

VM WEB0#

VM WEB1#

VM MAB0_<8>

VM MAB1_<8>

DRAM_RST# 76 77

INVENTEC

TITLE
MODEL PROJECT FUNCTION

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 75 of 77



